GALLIUM ARSENIDE PILOT LINE FOR HIGH PERFORMANCE COMPONENTS

Contract No. F29601-87-C-0202

AT&T
Guilford Center
P. O. Box 20046
Greensboro, NC 27420

Semiannual Technical Report for October, 1987 through March, 1988

June 2, 1988

The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the U.S. Government.

Prepared for
DEFENSE ADVANCED RESEARCH PROJECTS AGENCY
DARPA/DSO
1400 Wilson Boulevard
Arlington, VA 22209-2308

AT&T

DARPA

CONTENTS

LIST OF FIGURES

LIST OF FIGURES
(Appendices)

GALLIUM ARSENIDE PILOT LINE FOR HIGH PERFORMANCE COMPONENTS

Semiannual Technical Report
June, 1988

1. Introduction (S. F. Nygren)

The Gallium Arsenide Pilot Line for High Performance Components (Pilot Line III) is to develop a facility for the fabrication of GaAs logic and memory circuit chips. The first year of this contract is now complete, and this report covers the period from September 21, 1987, to March 27, 1988. Also included with this report are several items that are due at the end of the first year, as specified in Statement of Work (usually Section 6.2).

- Completion of the Pilot Line facilities and implementation of process controls (SOW 4.1.1). See Appendix A.
- Availability of the Pilot Line to process one lot per month in a foundry mode (SOW 4.4.1). See Section 3.6.
- A plan for increasing throughput in the Pilot Line (SOW 4.4.1). See Appendix B.
- A plan for evaluating yield trends (SOW 4.4.1). See Appendix C.
- Design rules, device terminal characteristics, and Process Control Monitors (SOW 4.1.4). This is being printed and bound separately, but it is being distributed along with this Technical Report.
- Industry survey of high speed packages (SOW 4.6.1). See Appendix D.

The User Friendly CAD System being provided by Hughes will allow outside users to design fully custom, standard cell, and cell array circuits for Pilot Line III. The AT&T Standard Cell Library, layout design rules, and simulation models have been entered into the appropriate tools. A preliminary demonstration was given at the Quarterly Review in January, 1988.

The planned sequence of Process Tester Chips is bearing fruit as simple circuits are used to develop models for use in more complex circuits. FETs from the PT-0 maskset were used to develop AC and DC model parameters at 25 and 125°C for nominal EFETs and DFETs statistically selected from PT-0 lot 3220. These models were used in the design of PT-1, a tester containing 49 small chips in each reticle field. These chips contained designs from AT&T Bell Laboratories in Reading and Cedar Crest and from Hughes. Logic designs were implemented in custom, standard cell, and cell array styles, and 256 bit SRAMs were also included. The first PT-1 processing lot was our first experience with 2μm line and space design rules along with two-level metallization. Fully functional circuits were obtained for all logic designs, and the best memory chip had 253 working bits out of 256. The logic circuits demonstrated 200MHz operation at the 15-20 gate delay design target. The successful convergence of a new process, new design rules, and new models into working circuits helps validate our approach of building a sequence of progressively more complicated circuits and

feeding the test results back to the modeling and wafer fabrication processes.

Our circuit simulation model has now been updated by including interconnect capacitances and information from the first six PT-1 wafers. This model agrees with PT-1 measured results within 30%, excellent agreement for this stage of development. In the future, the model will be refined to include best and worst case information. The present model information is being used in the design of two more tester chips (PT-2L and PT-2M) and the first full size standard cell circuit (Casino Test Chip). The logic circuits in PT-2L and PT-2M continue the exploration of the three design styles and include circuits over 2000 gates. The PT-2M SRAM will be a clocked 256 bit part that can operate in either pipeline fashion or ripple through. Our 3.7K gate version of the Casino Test Chip is designed to allow comparison to a future cell array version of the same circuit. The existing models are good enough to give us confidence that all these circuits will work at 200MHz.

Excellent progress is also being made in developing a technology for manufacturing these devices. The MBE wafer supply has stabilized, with MBE-1 delivering 24 wafers per week to the Pilot Line for the past 9 weeks. The second machine, MBE-2, is now ready for production use. Reducing design rules to 2μm lines and spaces has reduced interconnect parasitics. Oxygen implant planar isolation has been implemented, and the processing window for the EFET etch has been widened by changing the procedure. Via and continuity testers on the PT-1 and PT-X masksets confirm that present circuit yields will not be limited by these features, but processing improvements may be needed for 5000 gate circuits. Laser programming has been successfully demonstrated, and the PT-2M SRAM will contain spare rows and columns to allow circuit repairs. True high speed packages have been identified for the PT-1 chips and all of the SRAMs (TriQuint 24 signal / 44 total pins) and the PT-2 logic chips (Interamics 64 signal / 88 total pins). No high pin count, high speed package is available for the Casino Test Chip. It will be packaged in a 256 I/O fine pitch leaded flatpack designed by AT&T for the EMSP program, but the package will probably limit the chip performance.

FET response to transient radiation testing has been substantially reduced by placing a SiN layer beneath the metallization and by using a superlattice structure in the GaAs. This has allowed the characterization of a photovoltaic effect in which current flows into the gate and out the source and drain. SARGIC HFET ring oscillators have been subjected to 1×10^8 rad(GaAs) total dose. The average drain bias current decreased by 7%, and the oscillation frequency decreased by 4%. Single event transients caused by alpha particles in HFETs are reduced by more than an order of magnitude compared to MESFETs. Electromigration studies in a test structure from PT-0 extrapolate to a 3×10^6 hour time to failure at 200°C and 1×10^6 A/cm^2. Reliability at actual use conditions will be even better, of course.

2. Design

2.1 User Friendly CAD (L. R. Fisher, C. P. Heaney, M. T. Nguyen)

The development of the User Friendly GaAs CAD System to support the DARPA Pilot Line III made excellent progress along two fronts during this reporting period.

First, design capability was further developed in existing components of the CAD system. A cell library, layout design rules, and simulation models for the Pilot Line were entered into the appropriate tools. This information, in preliminary form, was used during the Third Quarterly Review to demonstrate:

1. Schematic Capture,
2. Logic Simulation,
3. Timing Analysis,
4. Circuit Simulation,
5. Standard Cell Automatic Place and Route,
6. Polygon Layout,
7. Parameter, Parasistic, and Circuit Extraction from Layout,
8. Layout vs. Logic comparison, and
9. Layout Design Rule Checking.

Second, several new tools have been or are being integrated into the CAD System.

N.2, an architectural simulator and design tool sold by Endot Inc., was integrated such that it uses structural information (schematics) in the CAD System and shares the user interface provided by the CAD System. N.2, as integrated into the GaAs CAD System, has been demonstrated to executives from Endot (with a favorable response!).

HITS, a test development tool available from the Naval Air Engineering Center, is currently being integrated into the GaAs CAD System. Several commercial Gate Array layout tools are also being evaluated for future integration into the GaAs CAD System. These include Mayo's MagiCAD, Mentor Graphics Gate Station, and Tektronix Merlyn-G.

Figure 1 illustrates the functional architecture of the GaAs CAD System. Table 1 lists the current status of cells from the AT&T standard cell library in the GaAs CAD System.

2.2 Demonstration Vehicles

2.2.1 Strategy (K. W. Wyatt)

One year after the start of the Pilot Line III project, design/modeling effort has delivered functional test circuits. To be seen in the subsections to follow are data from Process Tester Circuits with measured 200 MHz or better clock rate performance in a range of digital circuits of up to 0.46K gate complexity. This has been achieved through a development strategy, the successful implementation of which justifies confidence in the team's ability to deliver fully functional Pilot Line III demonstration vehicles, operating at the required speeds.

GaAs CAD SYSTEM ARCHITECTURE

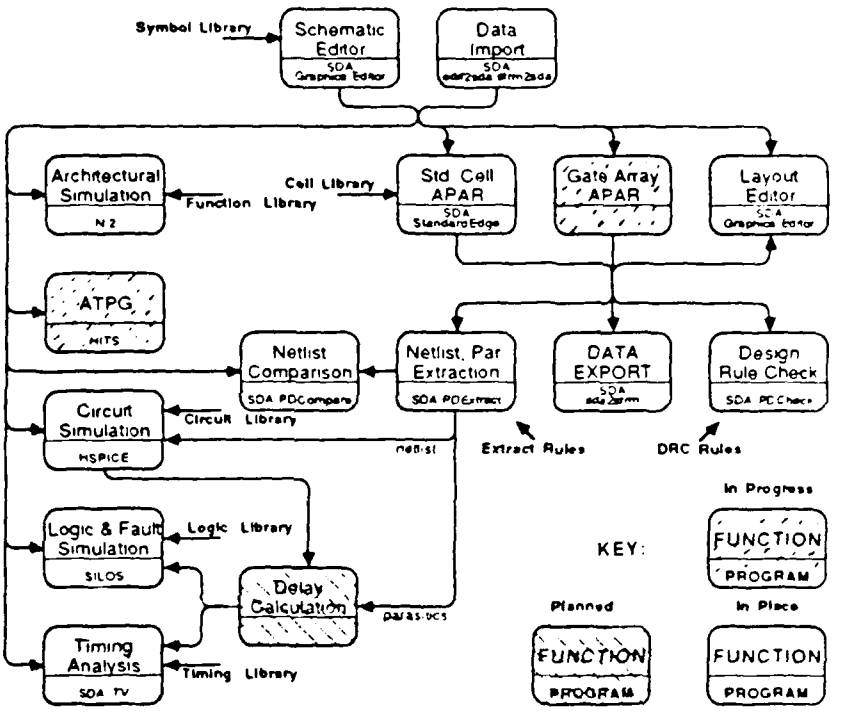


Figure 1. The GaAs CAD System.

Cell Name	Cell Function	Cell Layout	Cell Abstract	Cell Symbol	Schematic gate.sch	Circuit gaas.sch	N.2
bin01rlp	input pad	yes	yes	yes	yes	yes	yes
bin01tbp	input pad	yes	yes	yes	yes	yes	yes
bo75rlp	output pad	yes	yes	yes	yes	yes	
bo75tbp	output pad	yes	yes	yes	yes	yes	yes
ckdrv	clock driver	yes	yes	yes	yes	yes	
fd1s2ax	flip flop	yes	yes	yes	H	H	
fd1s2axg	flip flop	yes	yes	yes	H	H	
fd1s2dx	flip flop	yes	yes	yes	H	H	
fd1s2dxg	flip flop	yes	yes	yes	H	H	
fd1s2nx	flip flop	yes	yes	yes	H	H	
fd1s5f	flip flop	yes	yes	yes	H	H	
fd2s1cx	flip flop	yes	yes	yes	H	H	
feedthru		yes	yes	NA	NA	NA	
fill		yes	yes	NA	NA	NA	
gndpad	ground pad	yes	yes	yes	NA	NA	
gndpad_nc	ground pad	yes	yes	yes	NA	NA	
inrb	inverter	yes	yes	yes	yes	yes	yes
inrg	inverter	yes	yes	yes	yes	yes	yes
mux21	2 to 1 mux	yes	yes	yes	H	H	
mux21g	2 to 1 mux	yes	yes	yes	H	H	
mux41l	4 to 1 mux	yes	yes				
nd2	2 input nand	yes	yes	yes	yes	yes	
nd2g	2 input nand	yes	yes	yes	yes	yes	
nr2	2 input nor	yes	yes	yes	yes	yes	
nr2g	2 input nor	yes	yes	yes	yes	yes	yes
nr3	3 input nor	yes	yes	yes	yes	yes	
nr3g	3 input nor	yes	yes	yes	yes	yes	
nr4	4 input nor	yes	yes	yes	yes	yes	
nr4g	4 input nor	yes	yes	yes	yes	yes	yes
nr5	5 input nor	yes	yes	yes	yes	yes	
nr5g	5 input nor	yes	yes	yes	yes	yes	
oai22	or-and-invert	yes	yes	yes	yes	yes	
oai22g	or-and-invert	yes	yes	yes	yes	yes	yes
oai32	or-and-invert	yes	yes	yes	H	H	
oai33	or-and-invert	yes	yes	yes	H	H	
oai332	or-and-invert	yes	yes	yes	H	H	
sigdrv	driver	yes	yes	yes	yes	yes	
tbfin	tri-state buf	yes	yes	yes	yes	yes	
vddcor	corner cell	yes	yes	NA	NA	NA	
vddpad	vdd pad	yes	yes	yes	NA	NA	
xnor	exclusive or	yes	yes	yes	yes	yes	
xor	exclusive or	yes	yes	yes	yes	yes	
xorg	exclusive or	yes	yes	yes	yes	yes	

H = Described hierarchically (i. e., in terms of other cells in the library).

Table 1. Summary of GaAs CAD Standard Cell Library.

From its inception, four key (and interdependent) elements of the Pilot Line III contract had to evolve in parallel.

1) The MBE heterostructure device growth technique had to be transferred from research to manufacture and then proven-in.

2) The SARGIC HFET LSI processing technology had to be developed and demonstrated at AT&T's Reading location.

3) A modeling program, which began with the adaptation of an existing MESFET model and for which there was no initial data on the target SARGIC device, had to be used to provide design worthy heterostructure device models.

4) Given a process for which control windows are still narrowing, a standard cell library had to be developed for use in the design of a 3.7K gate logic circuit which will go to mask in mid-May of 1988.

The series of process testers (on masket sequence PT-X, PT-0, PT-1, and PT-2) were designed to study materials, processing, modeling, and design issues. The table below shows the original process test development plan

PLANNED PROCESS TESTER DEVELOPMENT	
INPUT	OUTPUT
Adapted MESFET model	PT-X, PT-0
PT-0; nominal, best & worst case models	PT-1
PT-1; nominal, best & worst case models	PT-2
PT-2; nominal, best & worst case models	Circuits A,D; 4K SRAM

However, without adequate data from which nominal, best case, and worst case models could be extracted from PT-0 and PT-1, the actual process development plan adopted is summarized in this table:

ACTUAL PROCESS TESTER DEVELOPMENT	
INPUT	OUTPUT
Adapted MESFET model	PT-X, PT-0
PT-0; nominal	PT-1
PT-0; nominal	PT-2, Circuit D
PT-1; nominal, best & worst case models	Circuit A, 4K SRAM

With the data available from the E- and D-FETs of PT-0, nominal devices were selected for purposes of extracting the parameters needed for simulations. This extraction occurred early in the third quarter of the contract. The characteristics of these nominal FETs agreed with those predicted from the device layer structure, doping profile, and aluminum profile. (The predicted threshold voltages, transconductances, and drain currents were determined from a self-consistent solution of the coupled, nonlinear Poisson-Schrodinger equations for the SARGIC HFET heterostructures.) These models were used in the design of PT-1 circuits which included logic circuits (of complexities ranging from a few tens of gates to 0.46K gates) and 256 bit

memory circuitry.

Because PT-1 test results were not available in time for PT-0 model revisions, the PT-2 logic and memory design proceeded (during the 3rd quarter of the contract) on the basis of PT-0 models. Similarly, Circuit D design has been completed on the basis of the nominal PT-0 model. (Circuit D, the Hughes 3.7K gate Casino test chip, will go to mask on May 15, 1988.)

FET data from the first 6 PT-1 wafers have been used to update the nominal model, and this updated model has been used to refine the PT-2 logic and memory designs. This PT-1 based model is the current model used in all simulations. It will be refined as necessary as more PT-1 data becomes available, and in October of 1988, the nominal PT-1 model will be replaced by one that is based on a statistically meaningful PT-1 FET database. Best and worst case models, base on PT-1 data, will also be made available in October of 1988.

Meanwhile, the 4K SRAM memory design has proceeded on the basis of the current (i.e., nominal) updated model, based on PT-1 data.

The existing PT-1 data is inadequate to justify rigorous comparison between simulation predictions and measurements. However, as of the end of the 4th quarter of the Pilot Line III Project, the existing PT-1 data does allow several conclusions.

1) The PT-series of masks has resulted in materials growth and process control sufficient to yield fully functional logic circuits, having 15 to 20 gate delays, which operate at better than 200 MHz clock rates.

2) The existing models are sufficient to provide the confident expectation that the 3.7K gate Casino Test Chip (Circuit D), which will be delivered on time, will be functional at 200 MHz. This expectation is based on the consistency of the measured and simulated results obtained at AT&T-Reading, AT&T-Cedar Crest, and Hughes. Despite different design approaches (semi-custom for Circuit D and for the Hughes PT-1 circuits; full custom for the Cedar Crest PT-1 circuits, semi-custom for the Reading PT-1 circuits), simulation and measurements agree to within better than 30% when interconnect capacitances are taken into account. For an immature technology, 30% agreement between simulation and measurement after 1 year of effort is more than encouraging. Granted, without best and worst case models, high yields are not to be expected. There is enough margin, nevertheless, to expect functionality at speed for the Hughes Casino Test Chip design.

3) Except for Circuit D, the DARPA III deliverable circuit designs will benefit from the availability of a statistically based model with best and worst case excursions. As a back-up design support plan, simulation of PT-1 circuits will be performed by using models extracted from FETs local to the chip sites. This will allow determination of the best and worst case models based directly on the actual yield of PT-1 wafers. By extracting local simulation models from FETs in the vicinity of tested chips (regardless of whether the chips are functional, marginally functional, or non-functional), measured ranges of model parameters will be available to generate best and worst case brackets around the nominal model parameters.

2.2.2 PT-1 Memory Design (M. V. DePaolis and W. R. Ortner)

Five memory test sites were designed for inclusion in the PT-1 mask package that was submitted to the shop on December 14, 1987.

Site1 - Basic 256-bit cell array tester with and without current limiting resistors.
Site2 - Rad-hard 256-bit cell array tester with and without current limiting resistors.
Site3 - Wordline driver and sense amplifier tester.
Site4 - Non-clocked 256-bit SRAM with basic resistor cell.
Site5 - Non-clocked 256-bit SRAM with rad-hard resistor cell.

Advice simulations were performed on all the circuits used in the PT-1 SRAM designs. In addition, a full chip model was used for simulating the overall performance of the 256-bit SRAM. Worst case analysis (1.8 V & 125°C) shows an address access time of 1.5 nanoseconds. Cell write time is only 0.5 nanoseconds. These values must be taken in context of the preliminary nature of the model files used for the simulations.

The testing strategy for PT-1 involves three levels of testing complexity. First, a basic parametric test set is used for measuring Sites 1, 2, and 3. Secondly, a 100 MHz functional bench set is used for testing Sites 4 and 5. This set allows internal probe capability and flexible input signal control. Finally, a fully automated Teradyne J937 test system is used to test sites 4 & 5. The Teradyne offers the most flexibility and characterization capability. Using address multiplexed timing, the Teradyne can achieve a 250 MHz maximum cycle rate.

The first wafer (11214) from the first lot of PT-1 testers utilizing AT&T's SARGIC HIGT GaAs process technology yielded one memory tester with 101 functioning memory cells. Three additional wafers were tested. One of the three wafers, 11212, showed considerable activity. Twenty-four out of twenty-five sites had some functioning cells, and four sites had over 200 working cells. Extensive characterization revealed typical access times less than 3 nanoseconds and average power consumption of 85 microwatts/bit at 50 MHz cycle rate. Figure 2 shows the access time map for a 253-bit functional site. Peripheral circuit current (IDD) and memory array current (IDDA) are plotted in Figure 3. Characterization of wafer 11212 at 200 MHz has begun.

2.2.3 PT-1 Design and Results (AT&T Logic) - (Y. K. Lo, W. A. Oswald, and E. K. Poon)

Three logic circuits were designed and included as reticle sites of the PT-1 test chip. These include a full custom 6x6 multiplier, a standard cell 4-bit adder, and a cell array ring oscillator. The speed goal is to achieve operation with a 200 MHz clock using a pipelined design with 15-20 cascaded gate delay stages (i.e., gate delays less than 250-333 ps). Preliminary test results show all three chip designs are fully functional. Based on the gate delay measurements from these three designs, the 200 MHz clock rate requirement is satisfied. PT-1 results demonstrate the GaAs technology and E/D SFFL logic family are favorable for implementing large scale integrated circuits. In the context of the new process line, new logic family and new design methodology, we have accomplished an important step toward the success of the

ALL Access Time Map - NS

0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f	
2.8	2.7	2.4	3.3	2.6	2.4	2.5	2.4	2.7	2.9	3.0	2.7	2.5	2.4	2.4	2.5	f
2.7	2.6	2.3	2.8	2.3	2.2	2.3	2.3	2.5	2.8	2.8	2.6	2.3	2.3	2.3	2.5	e
3.0	2.8	2.4	3.4	2.6	2.6	2.6	2.6	2.9	3.0	3.1	2.9	2.5	2.4	2.4	2.5	d
2.7	2.6	2.3	3.3	2.5	2.2	2.4	2.4	2.7	2.8	3.3	2.7	2.3	2.3	2.3	2.2	c
3.4	2.9	2.6	3.8	3.0	2.6	2.7	2.6	3.0	3.2	3.0	2.8	2.5	2.4	2.4	2.5	b
2.8	2.9	2.2	3.3	2.5	2.3	2.3	2.3	2.9	3.2	2.8	2.4	2.3	2.3	2.3	2.3	a
3.7	3.1	2.7	3.5	2.8	2.6	2.7	2.8	3.0	3.0	3.8	3.1	2.8	2.4	2.4	2.7	9
2.7	2.8	2.3	3.4	2.5	2.2	2.3	2.2	2.1	2.9	2.9	3.0	2.3	2.0	2.3	2.3	8
3.0	3.1	***4	3.8	2.9	2.6	2.5	***4	2.9	3.4	3.8	3.3	2.6	2.6	2.4	2.4	7
2.7	2.8	2.2	3.7	2.5	2.2	2.2	2.2	2.6	3.1	3.0	2.8	2.2	2.2	2.2	2.2	6
3.0	3.0	2.1	3.6	2.6	2.6	2.5	2.4	3.3	3.6	3.3	2.8	2.2	2.5	2.1	2.2	5
2.7	2.5	2.1	3.4	2.2	2.2	2.0	2.2	2.6	2.7	2.6	2.6	2.2	2.2	2.2	2.2	4
3.3	2.7	2.1	3.8	2.6	2.6	2.6	2.6	2.9	3.3	3.8	3.1	2.1	2.1	2.6	2.6	3
2.2	2.1	2.1	3.3	2.1	2.1	2.1	2.1	2.6	2.7	2.8	2.7	2.1	2.1	2.1	2.1	2
2.8	2.9	2.1	3.3	2.7	2.1	2.1	2.1	3.0	3.0	3.1	2.8	2.6	2.6	2.6	2.6	1
1.5	1.6	1.7	***4	1.8	1.8	1.8	2.0	1.6	1.7	1.6	1.8	1.8	2.0	2.0	2.0	0

AE AE[0] = 253 AE[1] = 0 AE[2] = 0 AE[3] = 0 AE[4] = 3 AE[5] = 0

AS Cnt = 253 Min = 1.48 Max = 3.75 Avg = 2.58 Sdev = 0.45

Die_X 33 Die_Y 17 Wafer 11212

Note. ***4 indicates non-functional cells.

Figure 2. Access Time Map for PT-1 Memory Site (33,17) on Wafer 11212.

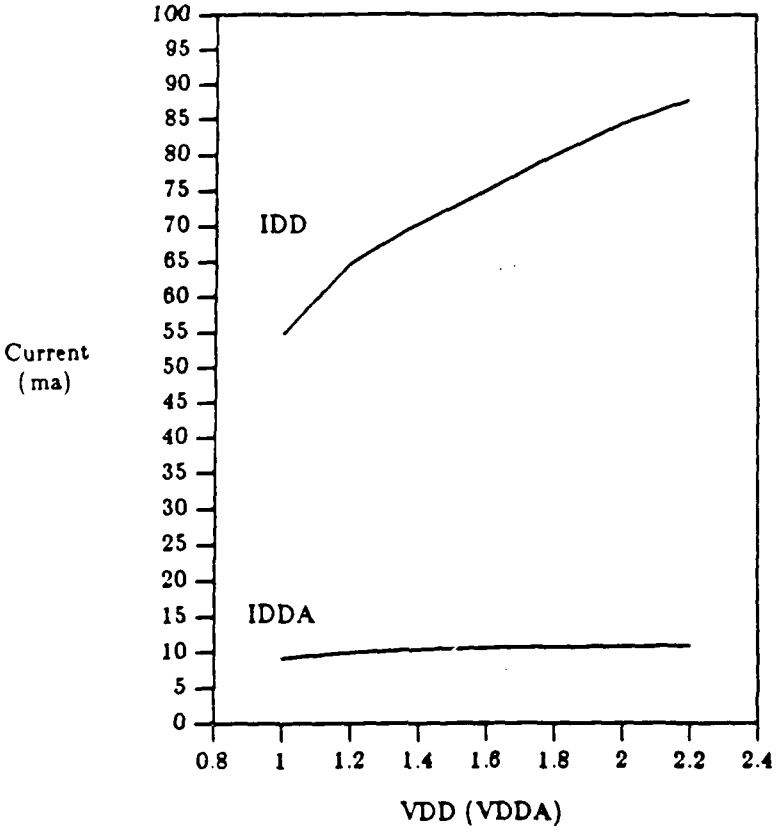


Figure 3. Average Current for the Six Best PT-1 Memory Sites on Wafer 11212.

DARPA III program.

6x6 Multiplier

The multiplier was designed 1) to obtain initial results on the design and fabrication capabilities of the GaAs technology for LSI circuits; 2) to prove-in the E/D SFFL family; and, 3) to verify new Gate Matrix CAD tools which are tailored for GaAs IC design. The functionality of the multiplier is based on the Baugh-Wooley two's complement multiplication algorithm. The circuit was implemented with E/D SFFL logic family and designed with a full custom approach.

One of the major reasons for choosing the multiplier design is its modular and repetitive architecture. The design makes it possible to pack more than 3000 transistors into the PT-1 die area and demonstrates the GaAs technology for LSI circuits. The multiplier was realized with 3072 transistors (465 gates). The longest delay path has 32 gates. The logic gates and adders within the modules were optimized for speed and power dissipation. The complete circuit, including the extracted parasitics, was simulated using ADVICE circuit simulator.

To obtain optimal performance, the chip layout was hand-packed using the GaAs Gate Matrix CAD tools. The layout floorplan consists of 33 blocks. These blocks were carefully arranged to butt next to each other without using routing channels. This approach minimizes routing parasitics and reduces layout area. The layout was designed to fit into a 2.25 mm^2 die area. The multiplier layout is shown in Figure 4. A complete functional and timing verification was performed by GOALIE, MOTIS, and ADVICE tools. GOALIE was used to convert the layout from the geometrical data base back to a transistor level description that could be verified using MOTIS functional simulator and ADVICE circuit simulator.

Several wafers were received from the pilot line. The multipliers were tested on wafer using a probe card. The performance of the circuits were measured using 4096 test-vectors on Advantest T3340 automatic tester at 2 volts and 25°C. Initial test results show the chips are fully functional from 1.7 to 2.4 volts with a multiplication time of 7.0 ns, which is equivalent to a delay of 219 ps/gate at 0.92 mW/gate.

4-bit Adder

The adder was designed for much the same reasons as the 6X6 multiplier. In addition, the 4 bit adder is an excellent vehicle for testing the standard cell placement and routing system, LTX2, as it relates to GaAs design. The adder is a conventional full adder with carry look ahead. The layout was constructed using the standard cell library developed at AT&T. One additional output was added to the circuit which (when fed back to the input) will cause the circuit to oscillate. The circuit contains 550 transistors (72 gates), and the longest delay path has 11 gates. The adder was successfully constructed using LTX2 and was verified using GOALIE, and ADVICE.

The performance of the circuits was measured using 256 test-vectors on an Advantest T3340 automatic tester at 2 volts and 25 C. Initial test results show the chips are fully functional from 1.7 to 2.4 volts with an addition time of 3.12 ns, which is equivalent to a delay of 284 ps/gate. The static current cannot be accurately reported because the adder shares the chip with other circuits.

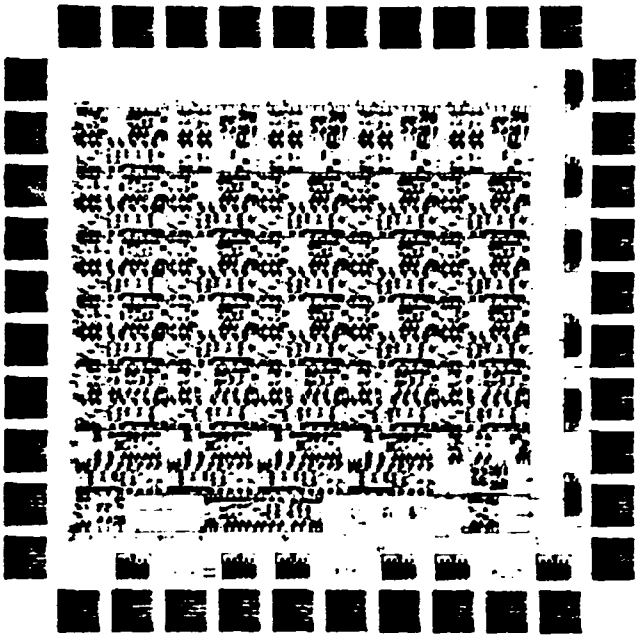


Figure 4 PT-1 6x6 Multiplier Layout

Ring Oscillator

This circuit consists of two ring oscillators, a 17-stage inverter ring oscillator and a 7-stage D-type flip-flop (with preset and clear) ring oscillator. Comcell is the basic structure of the cell array and is capable of implementing an INRG gate and a NOR-3 gate. Six Comcells, arranged in a 3X2 matrix, are used to form an island. Nine islands are used in the chip. The resulting circuit has 514 transistors.

Preliminary test results from five good sites show a 0.2 ns variation for the oscillation frequencies. The highest observed oscillation frequency for the flip-flop oscillator is 7.4 ns, or 135 MHz. The average propagation delay is 530 ps/flip-flop. Since the signal goes through three NOR-3 gates in the flip-flop, the delay for each NOR-3 gate is therefore 177 ps. For the inverter chain, the best observed oscillation frequency is 3.8 ns, or 268 MHz. The average propagation delay is 112 ps/inverter.

2.2.4 PT-1 Design & Results (Hughes Logic) - (A. Lee)

Hughes has designed four circuits for the PT-1 test chip. Each is a subcircuit of the Casino Test Chip, the 3.7K gate standard cell circuit that will be the first full scale logic chip designed under this contract. PT-1 is thereby used to pave the way for the full Casino Test Chip design. The Hughes PT-1 designs include: a 4-Bit Universal Shift Register, a 4-Bit Up/Down Counter, an 8-Bit Comparator, and a 16-to-1 Multiplexer. Shown in Figure 5, these range in complexity from 85 to 115 logic gates with the largest containing 682 transistors.

The ASIC design methodology used standard cells automatically placed in rows and routed

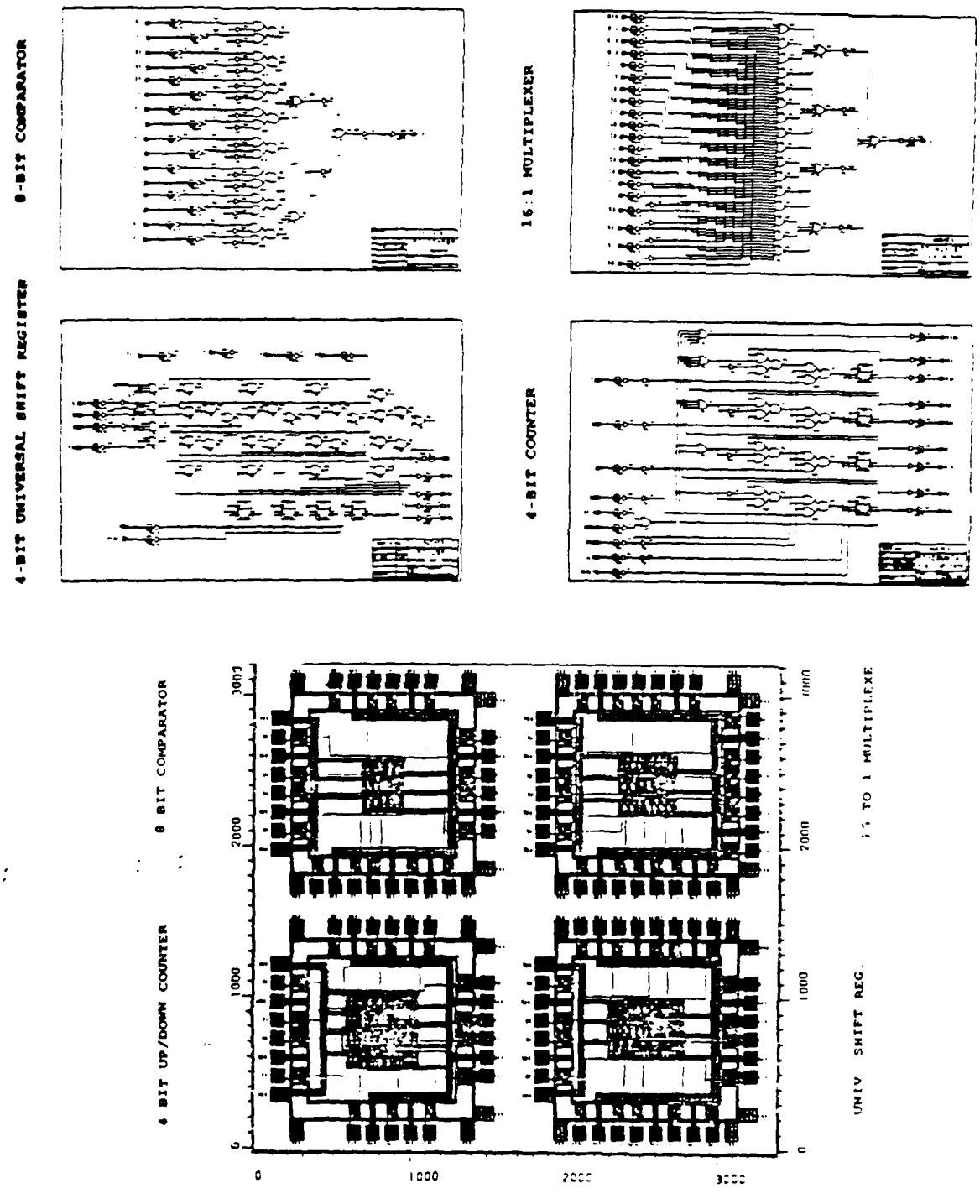


Figure 5. Logic Designs and Layout Designs for Hughes PT-1 Chips.

using commercial layout design tools. The designs were performed on Apollo workstations hosting Mentor Graphics (schematic capture and logic simulation), SDA (place and route), ECAD (layout verification), and HSPICE (circuit simulation) software. All CAD databases were populated with GaAs SARGIC/HFET process design rules, simulation parameters, and standard cell symbolic and layout libraries. This effort helped validate the approach used to design the Casino Test Chip.

As shown in the table below, all four standard cell designs were found to be fully functional on the first wafer lot. The sequential circuits were functionally verified up to 80 Mbits/sec, and the combinational circuits were measured to have 4.5 nS total propagation delays. Average dynamic power dissipation contributed by both the chip's internal core and I/O circuitry varied between the four designs from a low of 90 mW to a high of 142 mW.

PT-1 TEST RESULTS (WAFER #1)

Circuit	Yield	Dynamic Power	Timing Data
PT-1MUX16T1	11/25	102 mW	Prop Delay = 4.5 ns => 222 MHz
PT-1COMP8B	11/25	90 mW	Prop Delay = 4.5 ns => 222 MHz
PT-1USR	2/25	132 mW	Operates at > 40 MHz
PT-1COUNT4	1/25	142 mW	Operates at > 80 MHz

The following table shows the 1st set of DC functional yield data obtained from the first lot of wafers. The numbers represent a high success in first time functionality on the first GaAs processing attempt.

DC FUNCTIONAL YIELD

WAFER #	16:1 MULTIPLEXER	8-BIT COMPARATOR	4-BIT COUNTER	4-BIT UNIV. SHIFT REG.
11214	11/25	11/25	1/25	2/25
11205	6/25	8/25	2/25	3/25
11212	18/25	7/25	1/25	1/25
11206	7/25	9/25	1/25	0/25
11208	4/25	11/25	0/25	1/25
11204	13/25	6/25	0/25	0/25
AVERAGES:	**39%**	**35%**	**3%**	**5%**

2.2.5 PT-2M Memory Design (M. V. DePaolis)

The PT-2 memory design was begun in January. The PT-2 memory will be a clocked 256-bit

SRAM with several features and options. A block diagram of the clocked SRAM is shown in Figure 6. All memory inputs and outputs, except for Clock-In, will be latches which capture data on the positive going edge of the system clock. The design will also include laser programmable spare rows and columns. A "Mode" pin will be provided to control the operation of the data output buffer. The state of the "Mode" pin will determine if the output data is latched in a pipeline fashion or allowed to ripple through in the same cycle. The Output Enable Bar (OEB) controls the state of the data output driver. The output driver can be disabled, allowing the output pins of several packages to be wire-ORed. It is intended that all the peripheral circuit designs on PT-2 will be transferable to the 4K SRAM. Except for array size and organization, the PT-2 SRAM should emulate the operation of the 4K design. Mask shop date for the PT-2 memory design is May 6, 1988.

The memory design team has been in contact with McDonnell Douglas and the DARPA program office to discuss memory system interface and timing issues. First-cut memory features and timing diagrams have been sent to McDonnell Douglas.

2.2.6 PT-2L and PT-2M Logic Design (W. B. Leung)

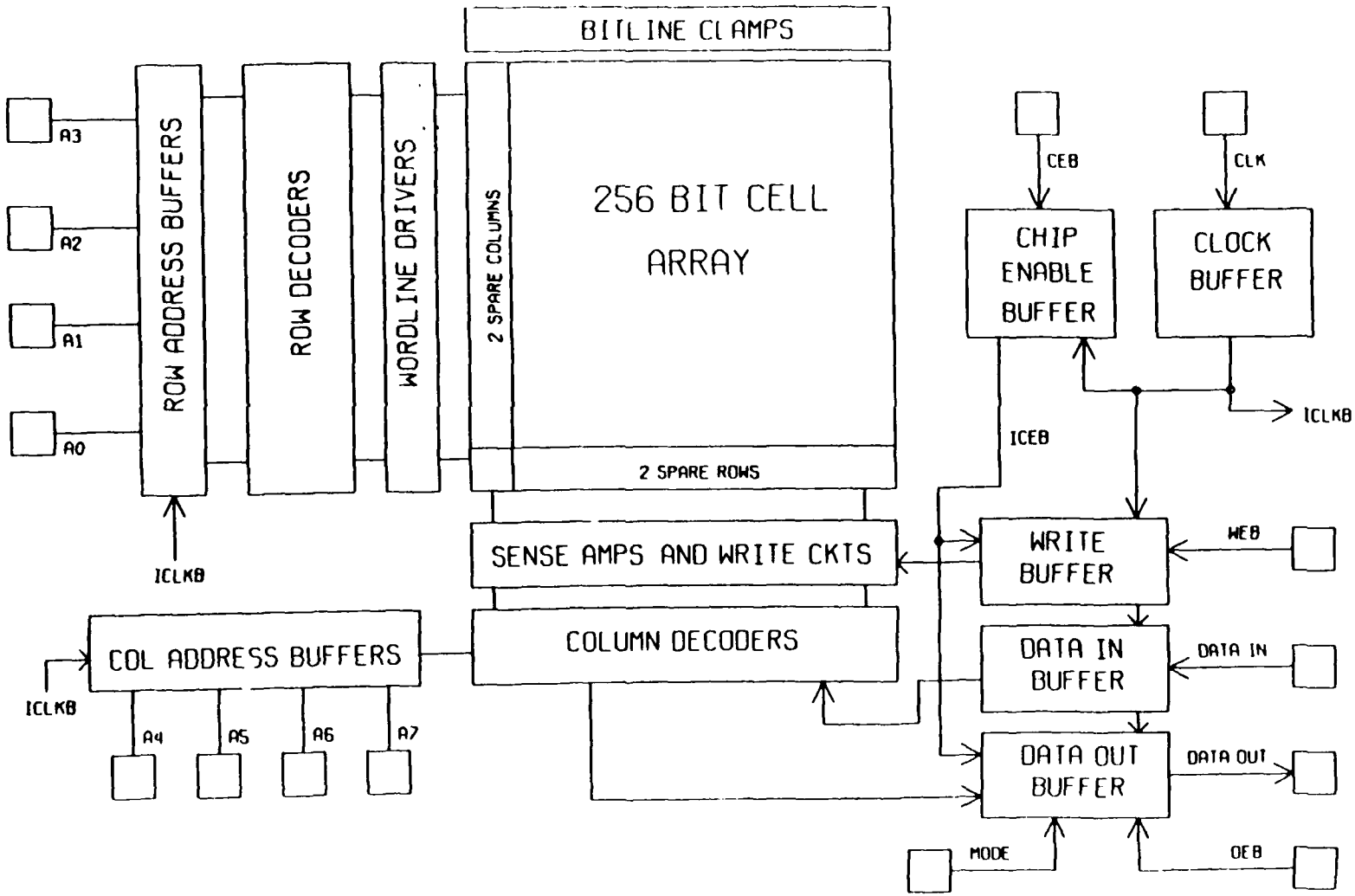
Six logic circuits are being designed for PT-2. The circuits, the source of the logic designs, the gate counts, and the their current status is shown in the table below. The four largest circuits will go into PT-2L, and the two smaller test circuits will go into PT-2M (which also contains testers for SRAM circuits).

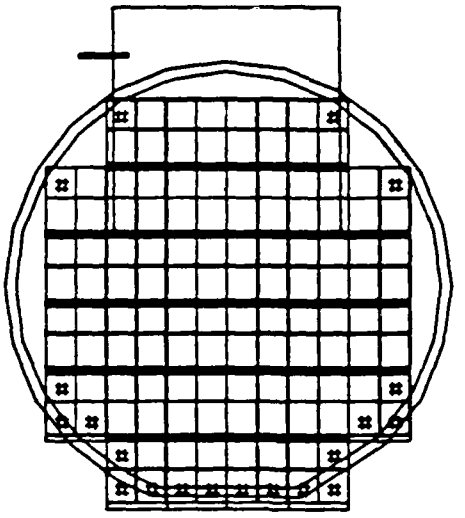
PT-2 Logic Test Circuits.

	Circuit	*Logic Design**	*Gate Count*	*Status*
PT-2L	ALU DEMO I	MDAC	2211	done
	Dual 8 x 8 Multiplier	ALC	1778	done
	Quad 4-Bit Adder	ALC	384	done
	Memory Tester	Mayo	1600	in progress
PT-2M	4-Bit Adder	ALC	96	done
	Programmable Multiplexer	ALC & RD	280	in progress

*MDAC = McDonnell Douglas, ALC = AT&T Bell Laboratories at Allentown-Cedar Crest, RD = AT&T Bell Laboratories at Reading.

The process tester PT-2L is implemented as a test vehicle for fairly large logic circuits with over 2k gate complexity. Smaller circuit blocks, from 100 to 450 gates, have been successfully processed in PT-1. PT-2L is intended to expand on the result of PT-1, and to include more functions in each circuit. This will enable the designers to verify their CAD tools, the modeling of circuit behavior, the process control over a large die size, and the yield characteristics. With consideration of the optimal reticle size, the die size of PT-2L is chosen to be 5.1mm by 5.1mm. Four distinct chips, together with a process control monitor, will be included in each reticle. Figure 7 shows the reticle sites and the number of chips on each 3 inch wafer.


BITLINE CLAMPS
A3
A2
A1
A0
ROW ADDRESS BUFFERS
ROW DECODERS
WORDLINE DRIVERS
2 SPARE COLUMNS
256 BIT CELL ARRAY
2 SPARE ROWS
ICLKB
SENSE AMPS AND WRITE CKTS
COLUMN DECODERS
COL ADDRESS BUFFERS
ICLKB
A4
A5
A6
A7
CEB
CLK
CHIP ENABLE BUFFER
CLOCK BUFFER
ICLKB
ICEB
WRITE BUFFER
WEB
DATA IN BUFFER
DATA IN
DATA OUT BUFFER
DATA OUT
MODE
OEB



NUMBER OF CHIPS PER FIELD = 4
NUMBER OF FIELDS = 32
NUMBER OF CHIPS = 108

Figure 7. PT-2L Wafer Array"

The ALU DEMO I is designed with the gate-matrix methodology. The logic design was done by McDonnell Douglas Corporation, and it consists of the ALU and the associated registers of a 32-bit microprocessor. Control signals and data path were included to facilitate the testing of the chip and the measurement of its characteristics. The dual 8 x 8 multiplier is an expansion of the 6 x 6 multiplier in PT-1. However, it is designed with the standard cell approach. Two multipliers were put into each die to increase the number of test circuits per wafer. This circuit will provide performance bench mark of the HFET processing and the SFFL logic family. The 8-bit multiplier has been fabricated in various processing technologies and logic families, and the results have been published in the past years. The quad 4-bit adder has the same logic function as the one in PT-1. However, it is designed in the cell array approach in PT-2L. Extra cell arrays were implemented to fill up all usable space, and it will be used to try out the cell array CAD tools developed by Mayo Foundation. The memory tester is also designed

with the gate-matrix methodology. This chip is the portion of the original Casino Test Chip that was removed by Hughes when the Casino Test Chip was re-architected for use in Pilot Line III (See Section 2.2.7). It can test up to 8 byte-wide SRAM's with up to 64k address space. The programmable multiplexer performs parallel to serial conversion with serial output up to 2 Gb/s.

The PT-2 test circuits encompass all three design styles as set out in the contract. Some of them are built from regular functional blocks, while others consist of mainly random logic. This combination of circuits should clearly demonstrate the reliability and reproducibility of the process, and the robustness of the logic family and design methodology.

2.2.7 Casino Test Chip Design (A. Lee)

During the six month time frame (October 1987 - March 1988) covered in this report, Hughes focused its attention on performing all the necessary tasks required to complete the design of the Casino Test Chip, also known as Circuit D.

The successful design, fabrication and test of four PT-1 logic circuits using HFET (Heterojunction Field Effect Transistor) SFFL (Source Follower FET Logic) technology, helped validate Hughes' ASIC design strategy, and paved the way for the complete design of the 1st full scale logic chip.

As part of this effort, a detailed primitive cell development effort was jointly undertaken by both AT&T and Hughes in order to establish a set of standard cells that were commonly usable by both pilot line designers and potential foundry customers. A total of 40 standard cells were designed, including NOR functions with up to five inputs, NAND functions with up to three inputs, and a number of OR-AND-INVERT (OAI) structures, flip flops, and higher complexity macrofunctions. Complete characterization of these was performed using the Hughes HSPICE circuit simulator and AT&T's SARGIC/HFET modeling parameters. Of these cells, 24 types (shown in Figure 8) were used to design the Casino Test Chip.

Furthermore, the Hughes Casino Test Chip was re-architected from its original 5k gate complexity to a 3.7k gate complexity version. This will allow the required comparison between the Hughes standard cell Casino Test Chip and a future AT&T cell array Casino Test Chip. (The cell array is required to be 5K equivalent gates; at 70% utilization, this is about 3.5K functioning gates.) Various enhancements were added to the Casino Test Chip, including the elimination of all gated clocks and the inclusion of board level testability via Boundary Scan techniques. Schematic capture and pre-layout functional simulations were performed to validate the design. The overall Casino Test Chip design is shown in Figure 9.

Layout of the Casino Test Chip was then performed using the SDA place and route software. This layout was subsequently analyzed and re-engineered using all known technical information extracted from the PT-1 design effort. Post-layout timing simulations were performed including all set-up, hold, and critical path delay times. Results indicate that operating frequencies in excess of 202 MHz (Hughes HSPICE GaAs models), and 213 MHz (AT&T ADVICE GaAs models) are achievable. These simulation results state that we can be optimistic of meeting DARPA's statement of work requirement of 200 MHz operation.

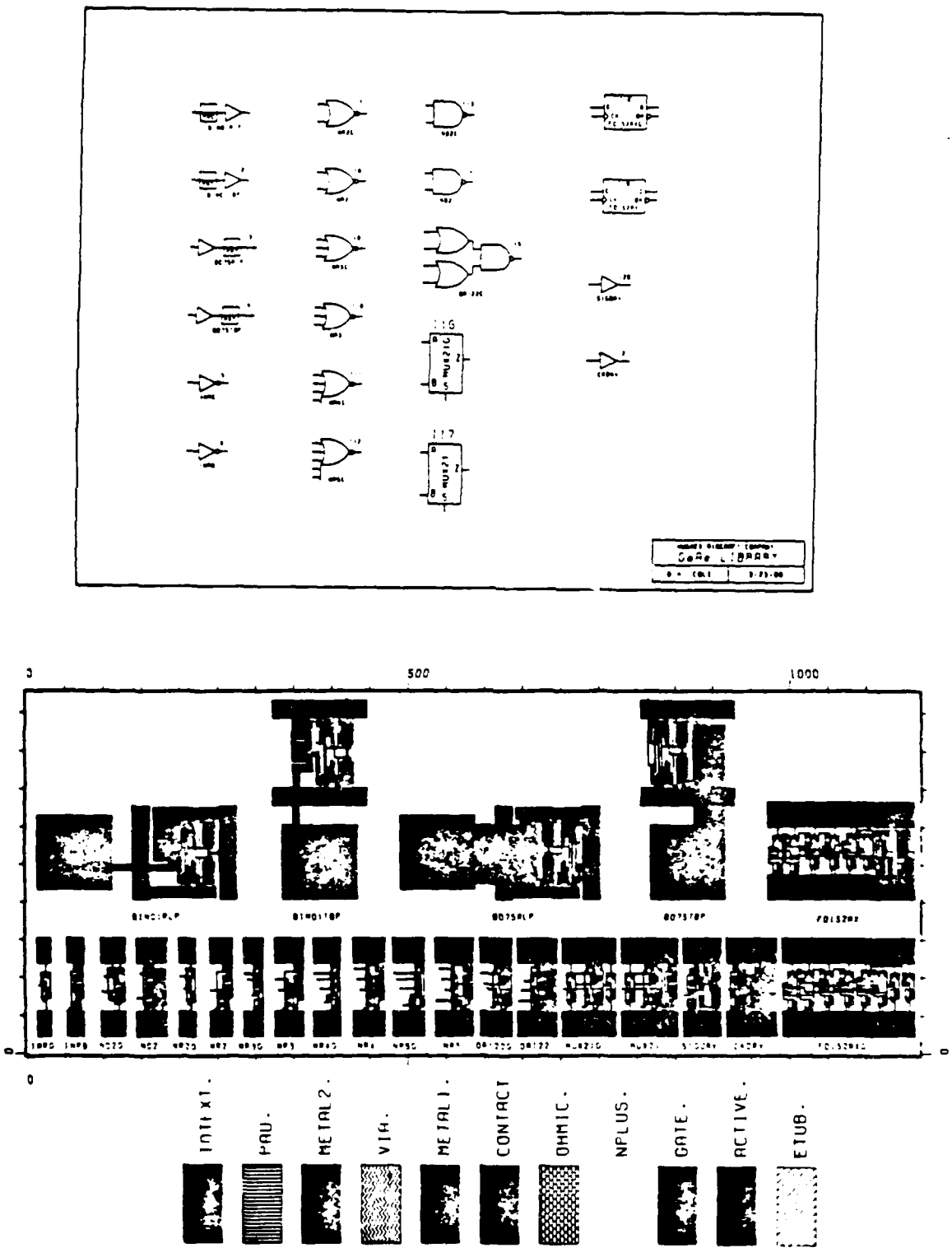
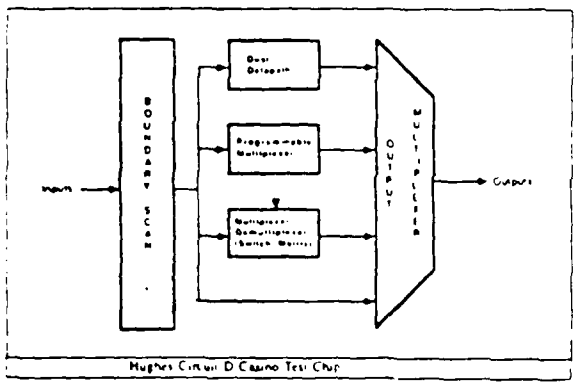


Figure 8. Standard cells Used in Hughes Casino Test Chip: Symbols and Layouts.



STATISTICS

- Fabrication Technology: AT&T SAIGIC/HFET 1.0, GaAs
- Power Supply Voltage: V_{DD} = 2.0 V
- Logic Family: SFFL (Source Follower Fet Logic)
- Complexity: ~3700 Gates (1 Gate = 6 transistors = unbuffered 2 I
- Layout Implementation: Standard Cell
- Number of Input Pins: 98
- Number of Output Pins: 74
- Number of VDD/GND Pins: 65
- Total Number of Pins: 241
- Die Size: 327 x 337 mils²
- Package: AT&T Bell Laboratories 256 pin EMSP (Leaded Chip Ca
- Average Dynamic Power Dissipation: 5 t W
- Termination Impedance: 75 Ohms (to be handled off chip)
- Required Operating Frequency: 200 Mhz
- External Logic Swing: 1.0 V

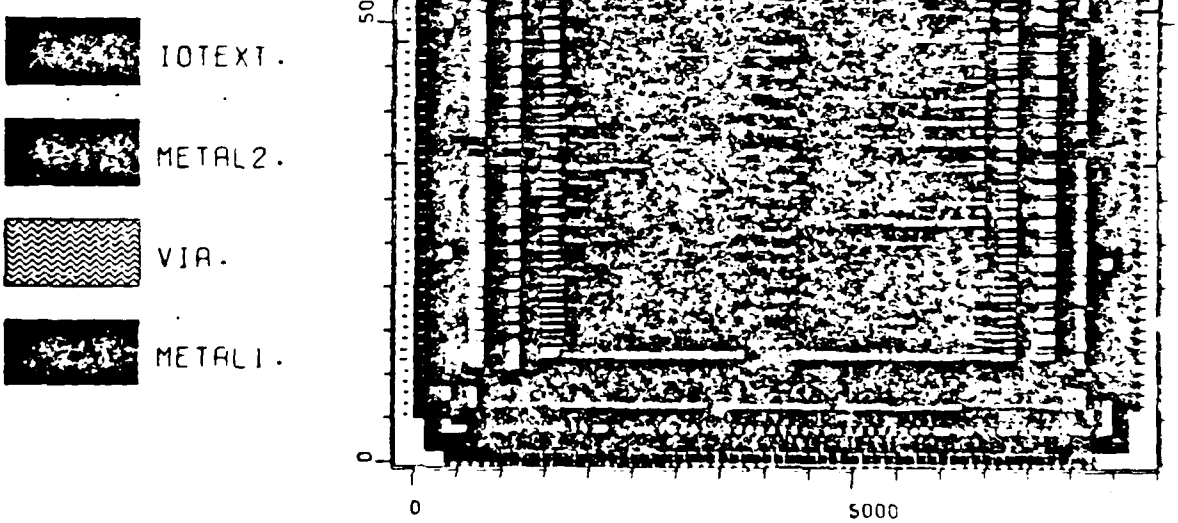


Figure 9. Hughes Standard Cell Casino Test Chip.

2.2.8 Laser Programming (R. T. Smith)

Two of the sites on PT-1 were allocated for design and evaluation of laser programming structures. LASERG1 is principally concerned with laser interactions with TOPMET (the upper level of circuit interconnect), while LASERG2 is aimed at laser interaction with BOTMET target structures. On each of these chips are four individual types of laser target structures connected to bond pads for electrical evaluation of continuity or open circuit status. Each of the four individual target structures is also replicated as a large array, also connected to bond pads for electrical evaluation.

Two of the features are designed to provide information on disconnecting circuit elements with the laser beam, one oriented horizontally and the other oriented vertically. In the corresponding arrays of these break-link targets, all links are connected in parallel and are separated by a TOPMET 'splash-fence'. The splash-fence is connected to bond pads for electrical evaluation of shorting from the break-links to the splash-fence after laser programming. The third target feature was designed to evaluate the feasibility of making a connection with the laser beam. The 'make-link' feature consists of two overlaid squares of interconnect separated by an interlevel dielectric. Two pulses are used to make the connection. The first is intended to explode a hole through the top metal and dielectric. The second pulse is intended to melt and splash the underlying metal, creating a vertical short to the upper layer. The fourth structure tests the feasibility of lowering the series resistance of vias between interconnect levels. The corresponding array consists of a large number of series-connected vias between two interconnect layers connected to bond pads.

The first PT-1 wafer used for laser programming had no passivating layer. This made it similar to unpassivated silicon wafers used in conventional laser programming of redundant memories. Unexpectedly, this wafer indicated that no useful processing window for laser energy exists for the break-link process without passivation. The gold metalization, whether BOTMET or TOPMET, horizontal or vertical, could not be reliably disconnected by the laser without significant shorting to the splash fence. Successful break-link processing requires a windowed passivation process to expose the target link metalization but provide a splash blanket over neighboring areas. This is illustrated for BOTMET in Figure 10. Two wafers with this windowed passivation were delivered to the laser group recently. Preliminary results from these wafers indicate a wide process window for laser pulse energy for horizontal link disconnect, whether BOTMET or TOPMET. The threshold energy is somewhat lower for BOTMET. Unfortunately, the process window for vertically oriented links is narrower and begins at roughly double the threshold energy (3 uJ or more), resulting in sporadic excessive damage to neighboring areas. This orientation dependence has been observed to a lesser degree in aluminum and other link materials and will be studied further. Clearly, designers should use horizontal link placement.

Results from the 'make-link' structures indicate that vertically shorted connections of a few ohms can be achieved with the double pulse technique, but considerable debris is generated in the process. Using the laser in CW mode, the via structures were irradiated at various energy levels without much success in terms of reducing the already low resistance. Indeed, some vias were destroyed in the time-consuming process. Further work on these two structures has been shelved indefinitely in favor of more urgent concentration on 'break-link' work in preparation for PT-2.

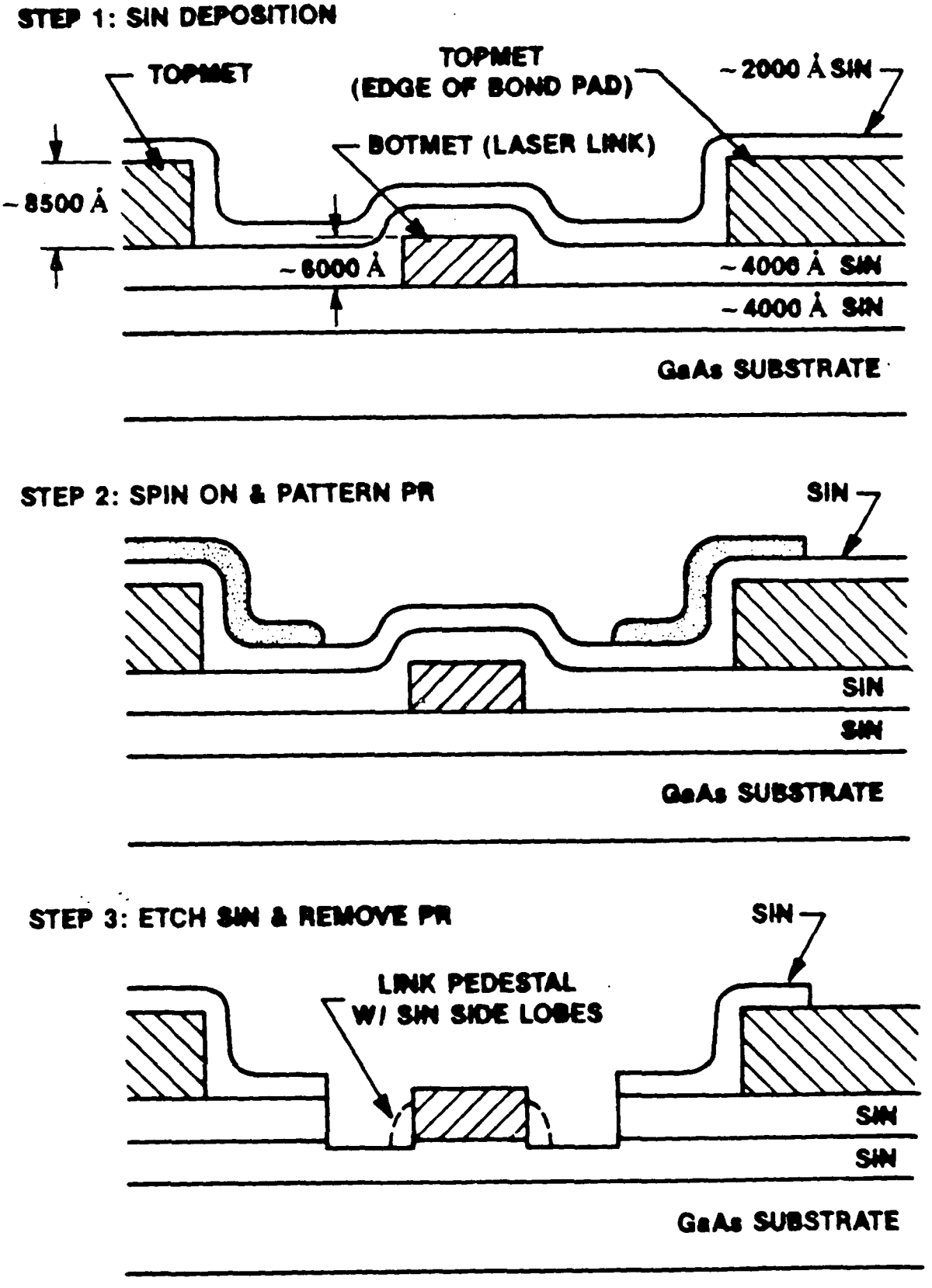


Figure 10. Cross-section of Laser CAPs Process.

2.3 Design Tools

2.3.1 Logic Family Validation (A. I. Faris)

The SFFL logic family is in the process of complete evaluation and testing. Initial results indicate SFFL gates will have a propagation delay of 90-110 pS and a power dissipation of 550μW. The AC noise margins will also be measured on certain gates. Initial results reveal the AC noise margins high and low are about 0.4V.

Simulations of AC noise margins for a DCFL and SFFL inverter were performed using AT&T's ADVICE circuit simulator. The simulations showed that SFFL AC noise margins degrade at a lower clock frequency than DCFL. However, over the frequency range of interest (200-400 MHz) SFFL AC noise margins are 4 times higher than DCFL. The simulations were done at 25 and 125°C. The simulation predicted a worst case AC noise margin of 0.4V, which agrees with the measurement.

2.3.2 PT-1 Standard Cell Library (A. I. Faris)

A standard cell library consisting of 37 cells was designed and layed out in the 2μm SARGIC/HFET process. The cells were incorporated into PT-1, and they are being characterized. Initial results indicate full functionality on all cells. Correlation between measured and simulated results will be reported on in the next technical report.

The following is a list of the standard cell library. At present they comprise the DARPA Pilot Line III standard cell library.

1. INRB, Inverter*
2. NR2, 2 input NOR gate*
3. NR3, 3 input NOR gate*
4. NR4, 4 input NOR gate*
5. NR5, 5 input NOR gate*
6. ND2, 2 input NAND gate*
7. ND3, 3 input NAND gate
8. OAI22, 2/2 input OR/AND/INVERT gate*
9. OAI32, 3/2 input OR/AND/INVERT gate
10. OAI33, 3/3 input OR/AND/INVERT gate
11. OAI332, 3/3/2 input OR/AND/INVERT gate
12. XOR, 2 input Exclusive OR gate*
13. XNOR, 2 input Exclusive NOR gate
14. MUX21, 2 to 1 Multiplexer*
15. MUX41L, 4 to 1 Inverting Latched output Multiplexer
16. DECOD, 1 to 4 output Demultiplexer/Decode

17. SIGDRV, Non-Inverting Signal Driver
18. CKDRV, Non-Inverting Clock Driver
19. TBFIN, Non-Inverting Tri-state Buffer
20. FD1S2AX, Negative Edge Trig. D Flip Flop*
21. FD1S2DX, Negative Edge Trig. D Flip Flop with positive clear*
22. FD1S2NX, Neg. Edge Trig. D Flip Flop with pos. clear and preset
23. FD1S2CX, Neg. Edge Trig. Master/Slave D flip Flop with Pos. clear and preset
24. FD1S5F, Neg. Level Trig. D Flip Flop with Pos. clear and preset
25. BINO1, Non-Inverting Input Buffer
26. BO75, Non-Inverting 75 OHM output Buffer

*These cells are available in both buffered and unbuffered versions.

2.3.3 Cell Array (T. C. Poon)

The 4-bit adder circuit of PT-2M was chosen to test the cell array methodology. It was chosen because the same circuit was already implemented in PT-1 with standard cells. Hence the performance and circuit areas can be compared directly.

The test chip also has another important goal. Since SFFL logic gates on the average have more transistors than other logic families, the SFFL logic circuits require larger areas. A good cell array design must therefore be able to implement complex logic gates with high fan-in's. However, complex gates with high fan-in's usually make routing more difficult to handle. We will use this demonstration to address these problems directly.

More routing spaces have been added to the PT-1 cell array basic structure (comcell) to make internal connections easier for the logic gates. One of the D-FET's in the PT-1 design is also changed to E-FET to make implementation of NOR-4 possible. Nine comcells are arranged in a 3X3 matrix to form an island. The purpose of using such an island is to make the circuit as compact as possible so that area comparison can be made with the standard cell circuit.

In the PT-2 layout, routing and interconnection were done manually since no well established CAD tools are available yet. However, the internal connection patterns of the logic gates have been personalized. The resulting circuit is actually fairly compact with about 70% usage of the comcells. The cell array adder requires an area of about 600μm X 1500μm, excluding the I/O frame. It is approximately twice the area of the standard cell circuit.

The ADVICE simulation results reveal no significant difference between the cell array circuit and the standard cell circuit. Therefore the actual performance of the cell array circuit is expected to be comparable.

Routing and interconnection are the major difficulties for SFFL cell array design. The design will depend strongly on the capability of the CAD tools used. Detail study of the layout indicates that if routing through the logic gates is not allowed, the island should be limited to a 2X2 matrix since most of the routing lines must go around the islands. The resulting circuit

would require 25% more area. The usage of the comcells would still be about the same for the 4-bit adder. But for circuits with much higher gate count, a smaller island would definitely be more desirable.

2.3.4 Parameter Extraction and Modeling (P. G. Flahive and R. D. Pierce)

PT0-based FET model parameters for the ADVICE 1M circuit simulator MESFET model have been established. Using global nonlinear least squares optimization techniques, DC parameters were extracted from measurements at 25C and 125C on nominal EFETs and DFETs statistically selected from PT0 lot 3220. Figure 11 compares the simulated DC characteristics with the experimental data at 25C. The fit at 125C is similar. Good agreement is obtained.

Some key DC parameters of the ADVICE model are listed in the following table.

Parameter	EFET		DFET		Unit
	25C	125C	25C	125C	
L	1	1	1	1	μm
VTO	0.20	0.13	−0.56	−0.58	V
MOB	1.1e4	0.6e4	1.2e4	0.9e4	cm^2/V-sec
VS	1.5e7	1.0e7	1.7e7	1.5e7	cm/sec
NSUB	1.0e17	1.0e17	1.0e17	1.0e17	cm^{-3}
PB	1.0	0.7	1.5	1.5	V
RO	440	410	480	340	Ohm-mm
RS	1.0	1.3	1.6	1.7	Ohm-mm
RD	1.0	1.3	1.6	1.7	Ohm-mm
ISS	3.7e−4	2.2e−3	1.2e−5	1.0e−3	mA/mm
ISD	3.7e−4	2.2e−3	1.2e−5	1.0e−3	mA/mm
N	2.3	1.8	4.0	3.7	--
PBRK	0.43	0.19	0.10	0.10	V

In this physically motivated model, L is gate length, VTO threshold voltage, MOB carrier mobility, VS saturation velocity, NSUB doping density, PB Schottky barrier height, RO output resistance, RS source parasitic resistance, RD drain parasitic resistance, ISS gate-source diode saturation current, ISD gate-drain diode saturation current, and N gate ideality factor. The parameter PBRK controls a rounding of the sheet charge vs. V_{gs} relationship near $V_{gs} = \phi_B$, and permits modeling the g_m compression seen in the EFETs.

The AC parameters were based on capacitances extracted from S-parameter measurements using a linear microwave model. This approach permitted a wider sampling of the bias space, and was first validated by comparing the derived capacitances with direct CV measurements. Reliable capacitance measurements could not be obtained at 125C, but the data suggested that the capacitances were not strongly temperature dependent, and the 25C capacitance parameters were also used at 125C. Figure 12 compares the simulated capacitances with the S-parameter results and with capacitances obtained from the physical modeling program of K. W. Wyatt. Reasonable agreement is obtained between the data, the circuit simulator model, and the physical model.

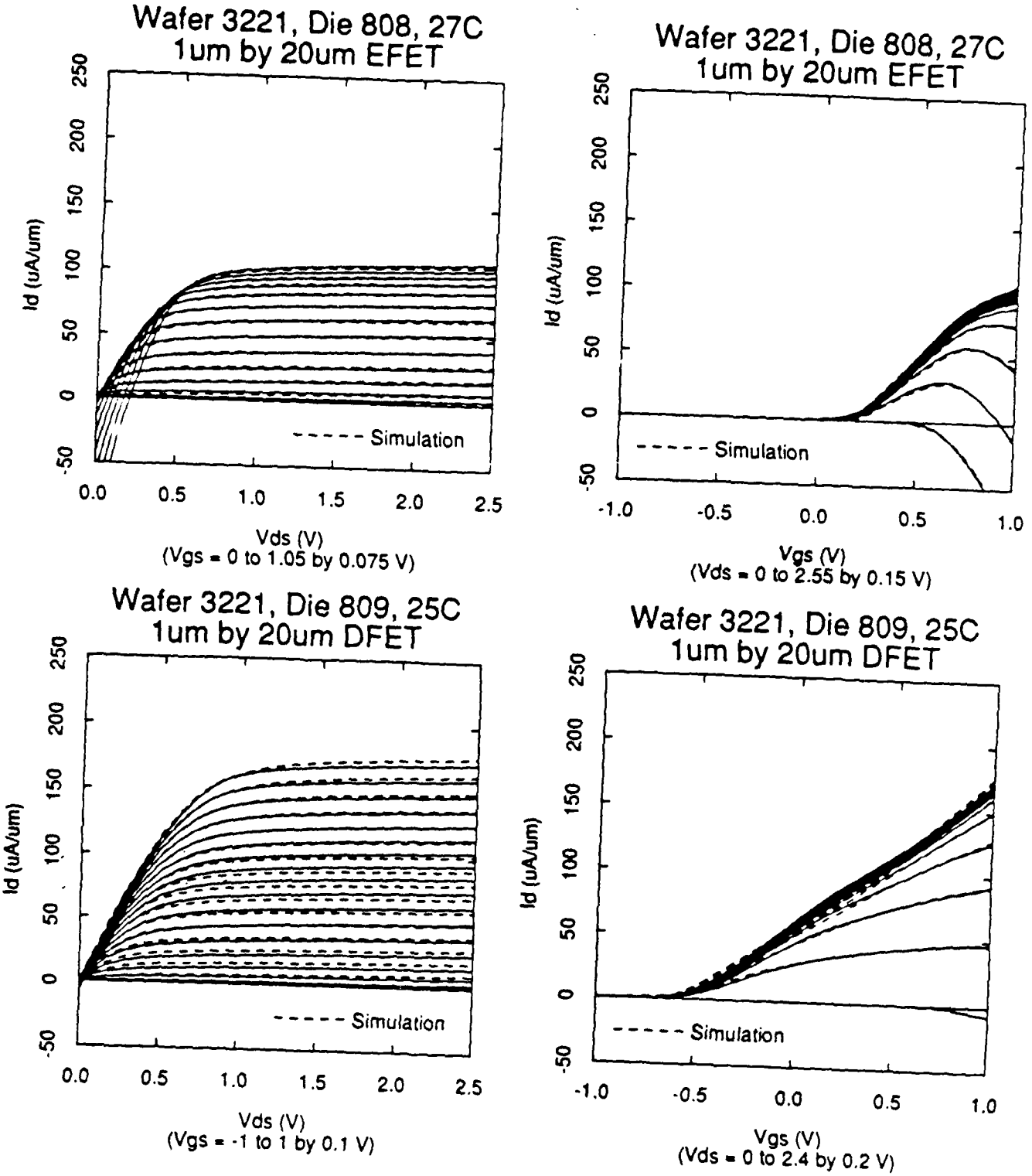


Figure 11. 25°C Measured and Simulated DC EFET and DFET Characteristics.

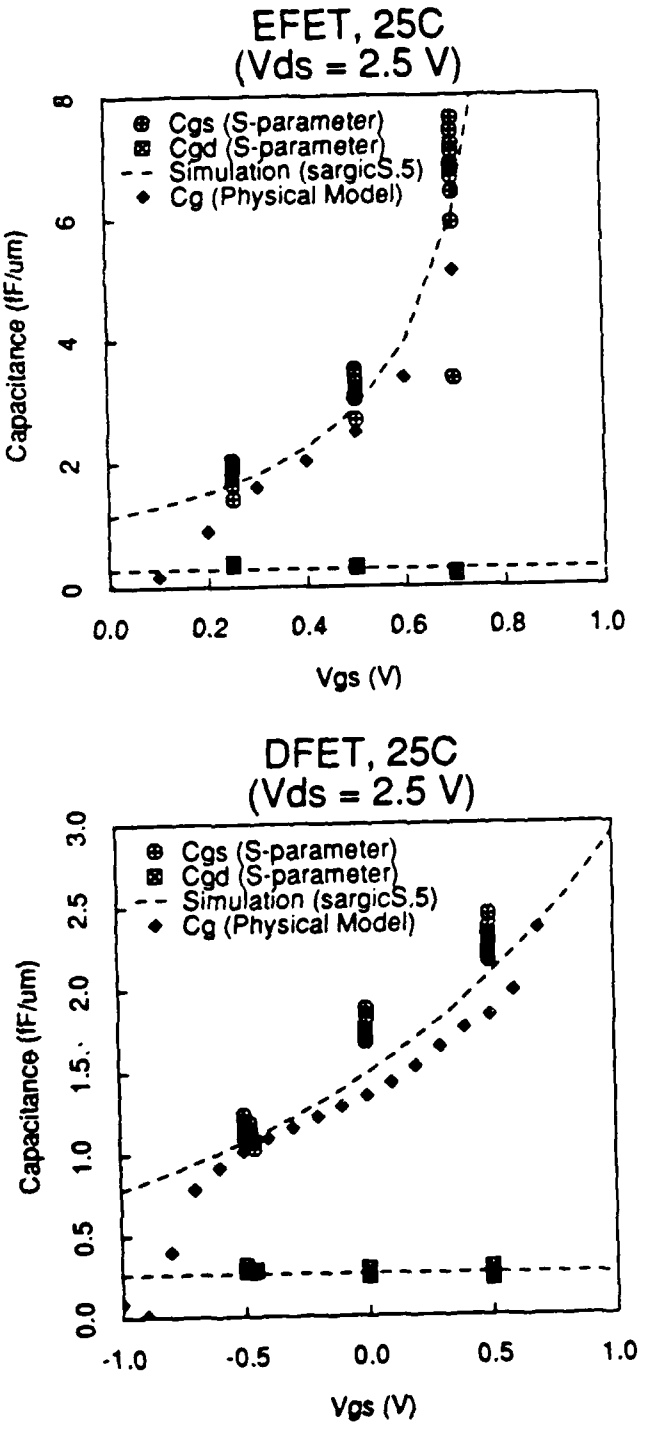


Figure 12. 25°C Measured and Simulated EFET and DFET Capacitances.

3. Pilot Production

3.1 Pilot Line Throughput & Interval (J. H. Duchynski, V. N. Patel)

Since the completion and certification of the GaAs LSI Pilot Line in February, 1987, all the required processing equipment have been installed, proved-in, and are being used for the development of the baseline E/D SARGIC HFET process. Installation and prove-in of additional facilities are continuing to improve the operating efficiency via increased automation (FSI Zeus Strip and Clean, and Process Products Solid Source Rapid Thermal Anneal) and increase throughput at gating operations (MBE Gen II, Temescal evaporator #2, a second Nikon stepper, SVG Photoresist apply tracks, and Testing).

Since November, 1987, lot starts, yields, interval and facilities have been managed using AT&T's computerized Shop Flow system. Additional information on the Pilot Line is included in Appendix A, including the statistical process controls being used on the line to improve the manufacturing discipline.

Figure 13 shows the continued increase in wafer starts for the last six months. Over 300 SDHT wafers were started with an average lot size of seven wafers. Our plan to increase throughput in the line is included in Appendix B.

Process Development interval for the 17 lots completed during the period averaged 48 days (Figure 14) - close to 3.5 times butt-to-butt interval. Butt-to-butt interval includes ohmic test but excludes final test. In order to reduce the processing interval, additional staff will be brought on line to selectively man the second shift for the critical operations such as MBE, testing, and photoresist.

Average wafer throughput yield for completed lots is 86% for this semi-annual period (Figure 15). Wafer throughput yield is the ratio in percent of the number of wafers delivered for PCM testing to the number of MBE wafers started in the Fab Line. Lower yield on Lot 15 resulted from misprocessing and the discovery of the sensitivity of selective etches for the definition of Enhancement and Depletion mode transistors. Newly introduced inspections will minimize the misprocessing while the etch sensitivity is being characterized to improve the process. Over 100 fully processed wafers were delivered for device modeling and testing from PT-0 and PT-1 reticle sets.

3.2 Baseline Technology (R. H. Burton, A. G. Baca)

During the last six months the focus of the baseline technology has changed from the resolution of fundamental device physics issues to a focus on issues related to manufacturability at LSI complexity. Ability to achieve design targets has again been demonstrated through the successful fabrication of working circuits on PT-1 such as the 6x6 multiplier. A number of advances have been made relating to manufacturability in the areas of interconnect technology, isolation, and E/D definition. The MBE program has continued to mature with more wafer deliveries and less equipment down time.

A reduction in interconnect parasitics has been necessary in order to achieve the stated circuit design speeds. A reduction in design rules from 3.5μm lines and spaces with 2.0μm vias to 2.0μm lines and spaces with 1.5μm vias has been achieved using liftoff with reentrant angle photoresist and evaporated gold. Development of a low stress, lower dielectric constant SiON film for interlayer dielectric insulation and passivation has been incorporated into the process. The via and interconnect process has been successfully tested using PT-X (described further in

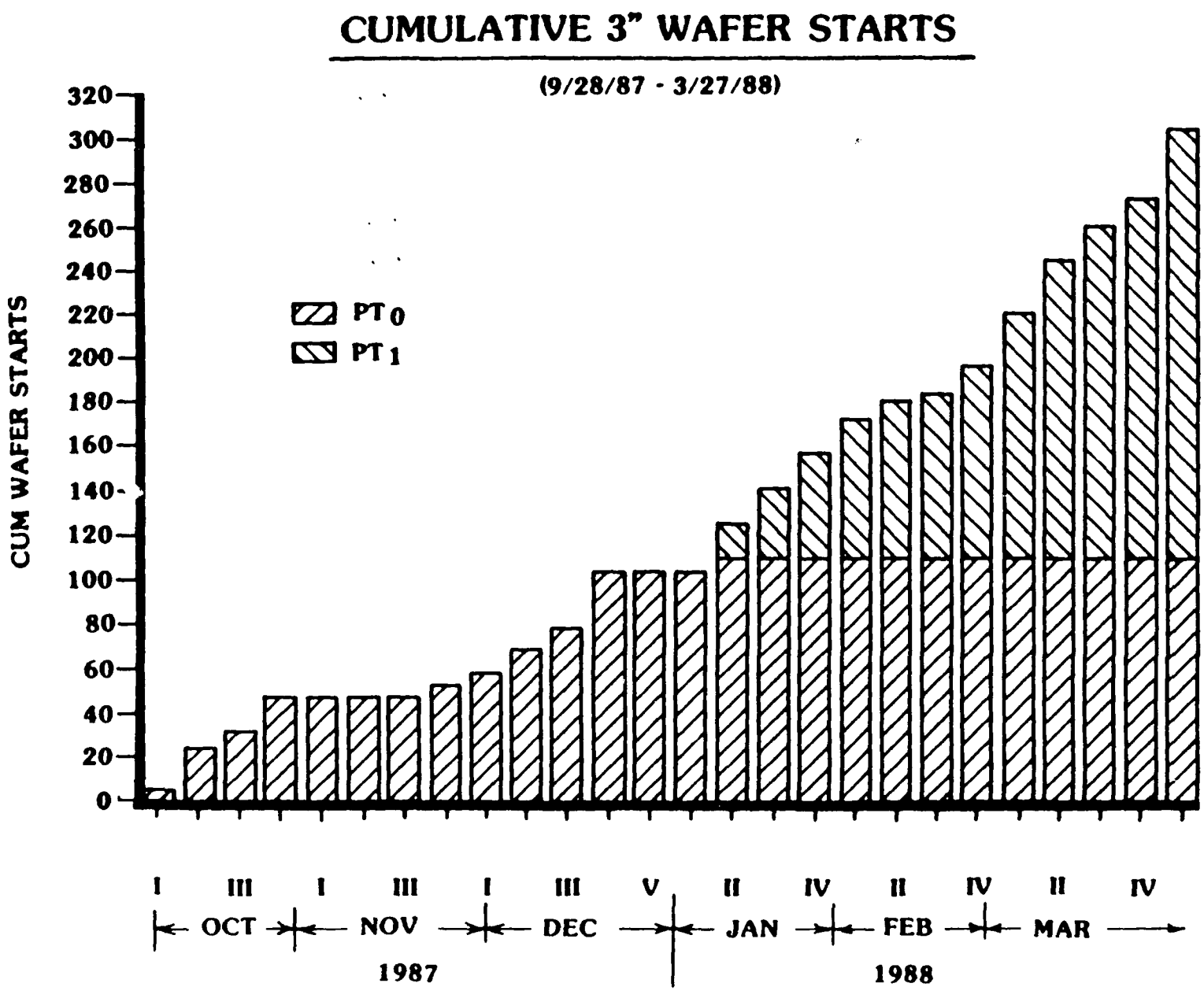
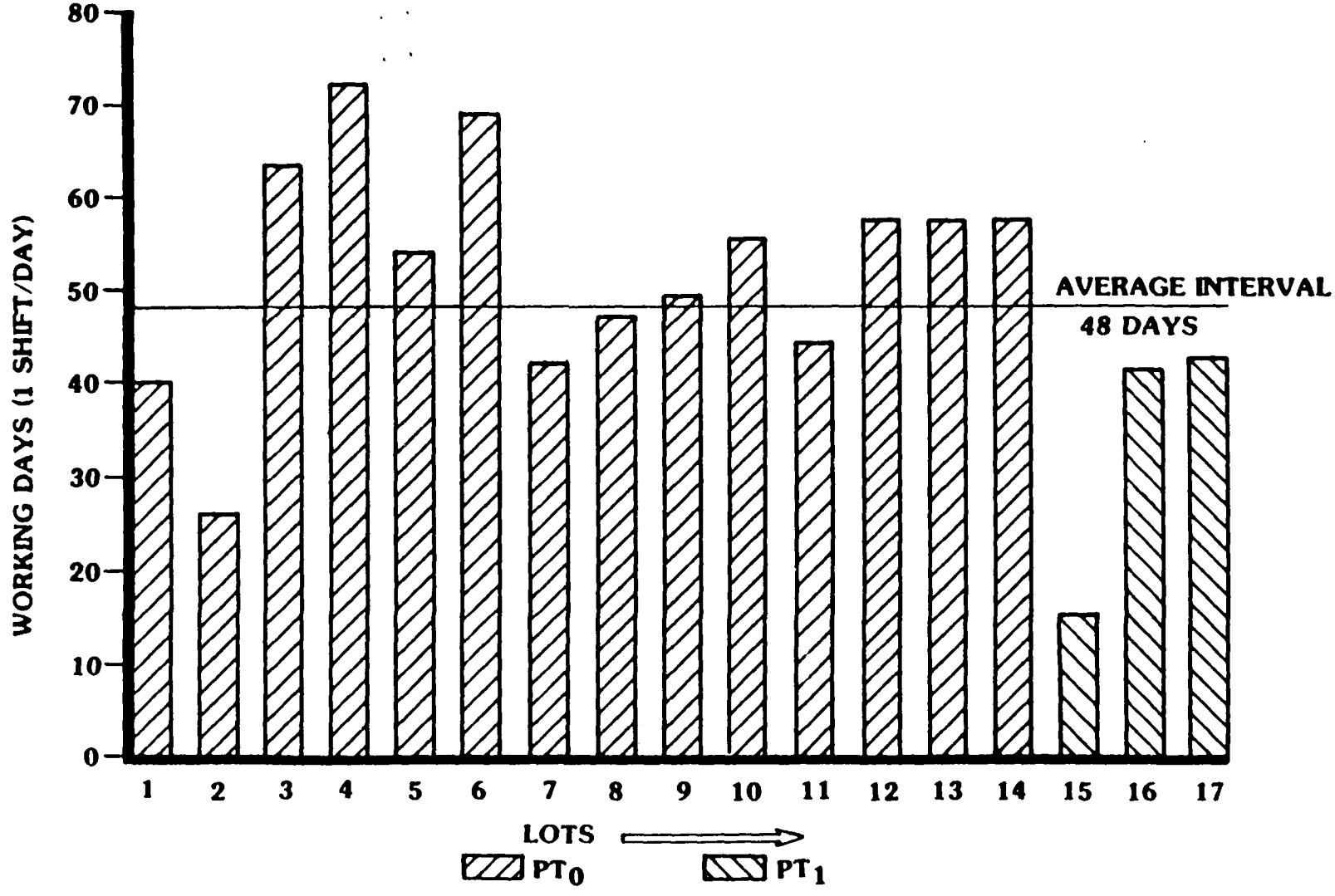


Figure 13. SARGIC HFET Wafer Starts

PROCESSING INTERVAL FOR DEVELOPMENT LOTS

(9/28/87 - 3/27/88)



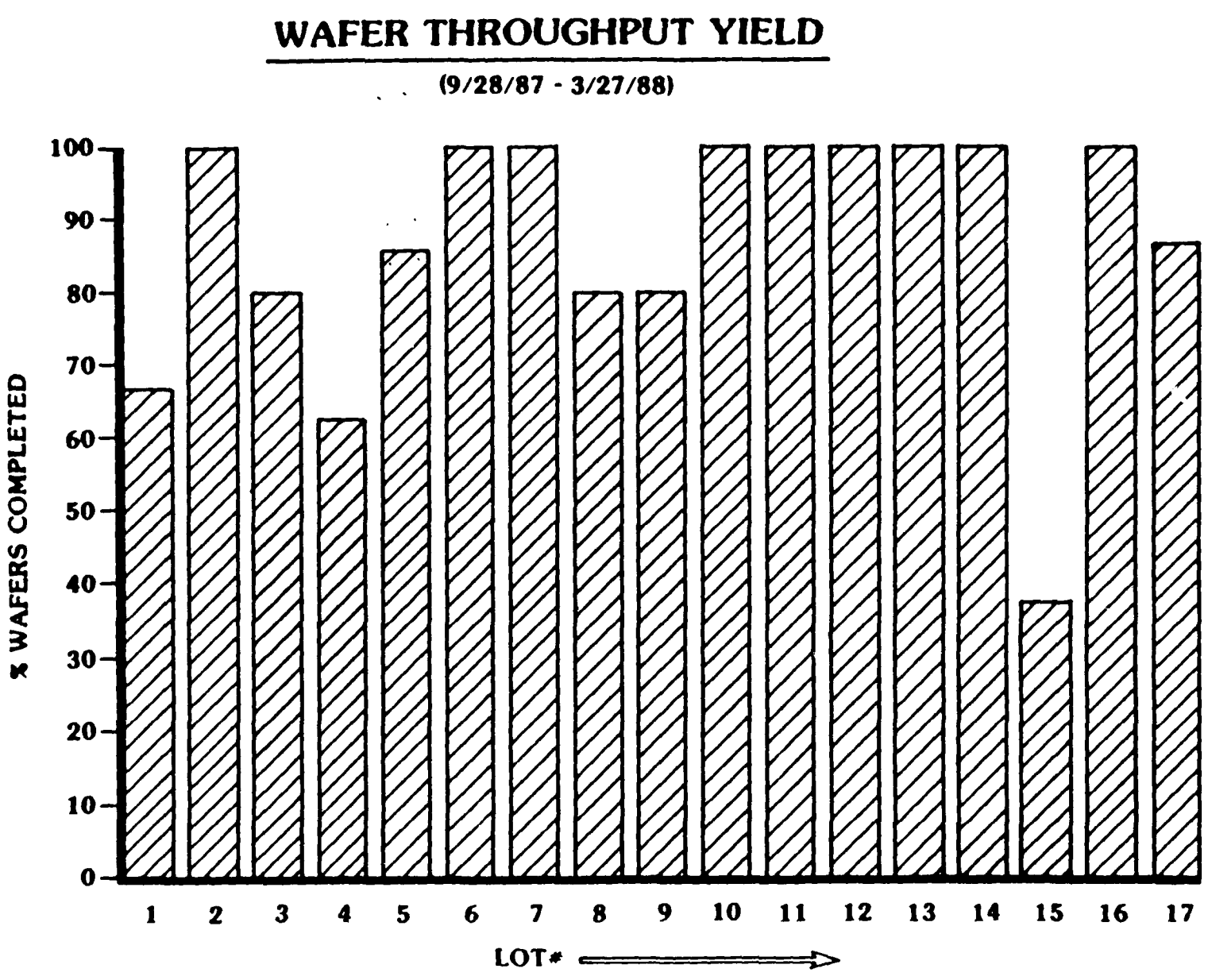


Figure 15. Wafer Throughput Yield for SARGIC HFET Completed Lots
(Wafers delivered for PCM testing Compared to MBE Wafers Started in the Fab Line)

section 3.3). The 2.0μm design rule process with two levels of interconnect was evaluated for the first time on PT-1. Several via testers were used to test the effect of extra morphology expected from the extral level of interconnects in the two-level metal process. Preliminary indications are that the via process is adequate for reasonable yields on PT-1 and PT-2, but that further improvements will be required for circuits of 5K gate complexity.

Other accomplishments during this period are as follows: A planar isolation process based on ion implantation of oxygen has been implemented. This achieves lower and more reproducible isolation currents than the mesa isolation method, and it survives the high temperature anneal. The planar process is important because it places fewer constraints on the photolithography and is expected to promote high yield. The EFET formation process window has been improved by means of a stronger HF solution and longer etch time in order to reduce the induction time recently observed in the AlGaAs etch. We have used TEM cross-section analysis to correlate E/D step height measurements with DC electrical characteristics for failures of the EFET etch. The gate turn on voltage, which has been a concern in the past, is reasonably consistent at .62 ± .05 V. Although a slightly higher value would be desirable, the currently quoted value is most probably fundamental to the process.

Progress continues to be made on the manufacturability of MBE. During the past six months, 372 wafers for Pilot Line III have been grown from MBE-1, averaging 15/wk. Deliveries for the most recent nine consecutive weeks have been at the 24/wk level, or essentially maximum output for MBE-1. Wafers have been grown from MBE-2 which have equivalent characteristics to MBE-1 as verified by Hall mobility, sheet charge, Rutherford back scattering, and device electrical characteristics. V_{th} standard deviation of EFETs is 22mV for four wafers processed from MBE-2.

Baseline technology efforts are now focussed on tightening process control, improving reproducibility, and carrying out failure mode analysis in key areas where yield improvement is expected. The interconnect process will be carefully evaluated to determine whether a 2μm design rule process based on liftoff and evaporated metal will provide sufficient LSI yields. Key areas such as MBE growth, the EFET etch, and gate formation will continue to receive major attention in order to improve reproducibility. In addition, MBE will focus on implementing RHEED oscillations into calibration procedures and ramping up growth capability from MBE-2. Finally, a major effort will be made in correlating material, process, device, and circuit characteristics.

3.3 PT-X (D. D. Manchon, M. P. Iannuzzi)

The PT-X process capability tester is a three level (Metal, Dielectric, Metal) mask set that has been designed to test product line process capability. The test circuits on PT-X have been primarily taken from National Bureau of Standards and Jet Propulsion Laboratories publications.

The types of circuits used are listed in the table below.

TYPES OF CIRCUITS ON PT-X

Y_o, D_o Testers For:	Metal Continuity Through Vias
	Metal Continuity for a Metal Layer
	Shorts Between Metal Lines
	Dielectric Isolation of Crossovers
	Dielectric Isolation of Capacitors
4 Terminal Contact Resistance Bridges	
Split Bridge Crosses	
(Patterns are laid out in orthogonal directions for 2.0 and 3.5μm design rules)	

Initial wafers were processed for a Ti/Pt/Au (0.6μm) top metal, SiN or SiON dielectric (0.4μm), and a WSi bottom metal (0.4μm). Results were obtained from seven wafers (two lots) tested at 40 or 45 sites per wafer.

The yield for vias in series using 2 and 3.5μm design rules are shown in Figure 16. The failure rate expected from vias in PT-1 circuits will be small because of the number of vias (maximum of 20,000) in these circuits. However circuits with several hundred thousand vias are expected to be developed near the end of the DARPA contract. It appears that some process improvement may be needed by this time to assure good via yields. In conjunction with via studies, studies of the contract resistance between metal layers are currently underway using four terminal bridges.

Yields for metal continuity, absence of shorts between parallel metal lines, and dielectric isolation of crossovers and capacitors are good. For metal serpentine lines 2μm wide and 10cm in length, the percent continuous for top and bottom metals is 97.6 and 99.8, respectively. The top metal serpentine crosses over the bottom metal 12,000 times. 97.5% of the top metal serpentines have no shorts to metal lines parallel to the serpentine lines and spaced 2μm away on each side of the serpentine. For the bottom metal, the yield is 95%. One poor wafer was responsible for reducing the yield from 98%. For future circuits occupying 1 sq. cm of area, there may be up to several hundred cm of metal lines on two levels. For this level of integration some process improvement may be required.

The dielectric isolation is excellent on the initial lots. Units of 100,000 crossovers have yields of over 98% for all crossovers being good. 97% of the capacitors with a total area of 3.4mm^2 have no shorts. At these yield levels, dielectric isolation would cause no significant yield problem in any planned circuits.

In a more recent experiment a bottom metal (Ge/Ni/Au) was used that was lifted off rather than plasma etched for delineation. Crossover isolation was not as good. See Figure 17. This is thought to be due to a small ridge left at the feature edge by the lift off process. The ridge punches through the dielectric. Further experiments have to be done to confirm this effect.

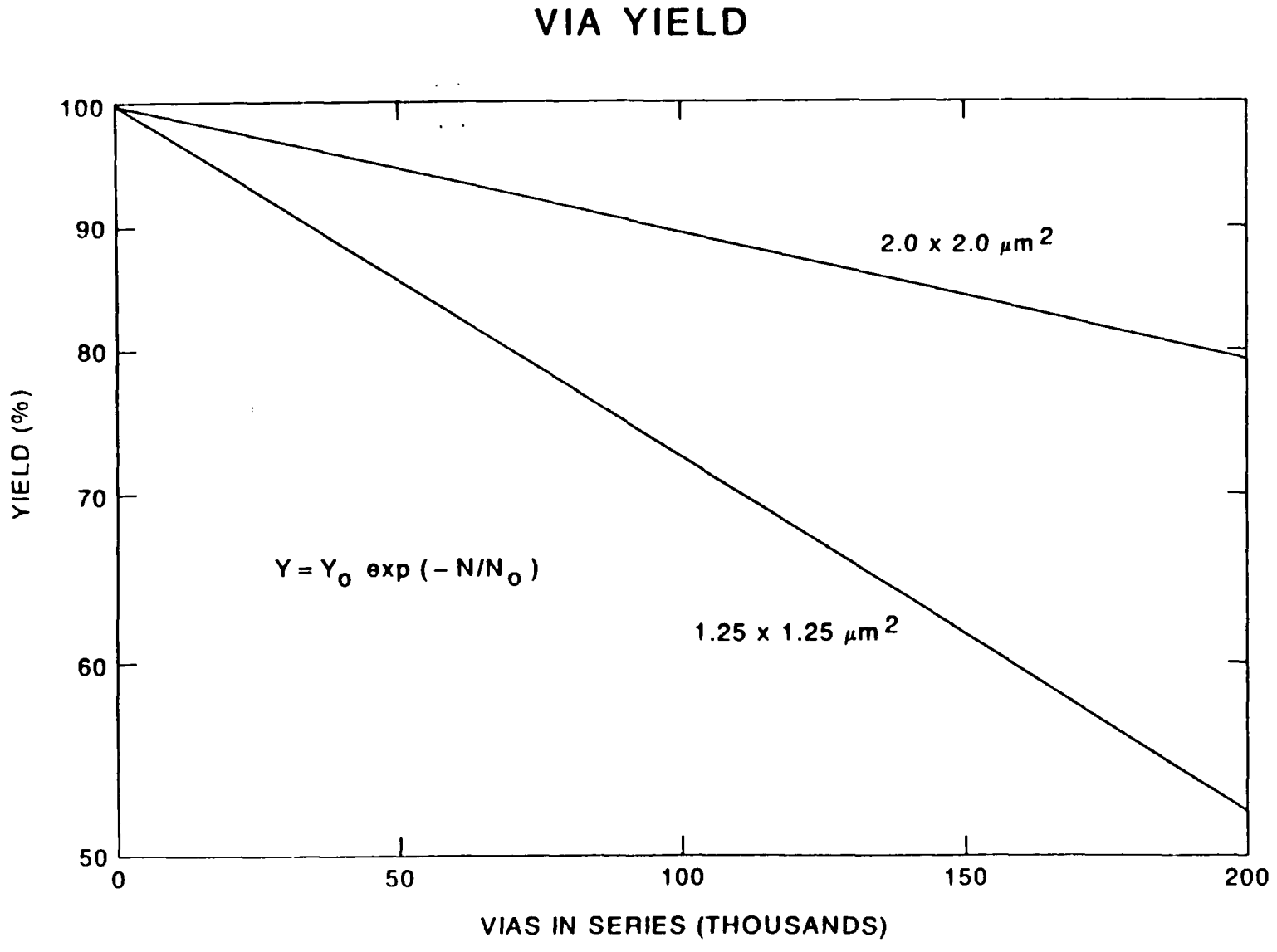


Figure 16. PT-X Via Yields for 2.0x2.0 um and 1.25x1.25 um Vias

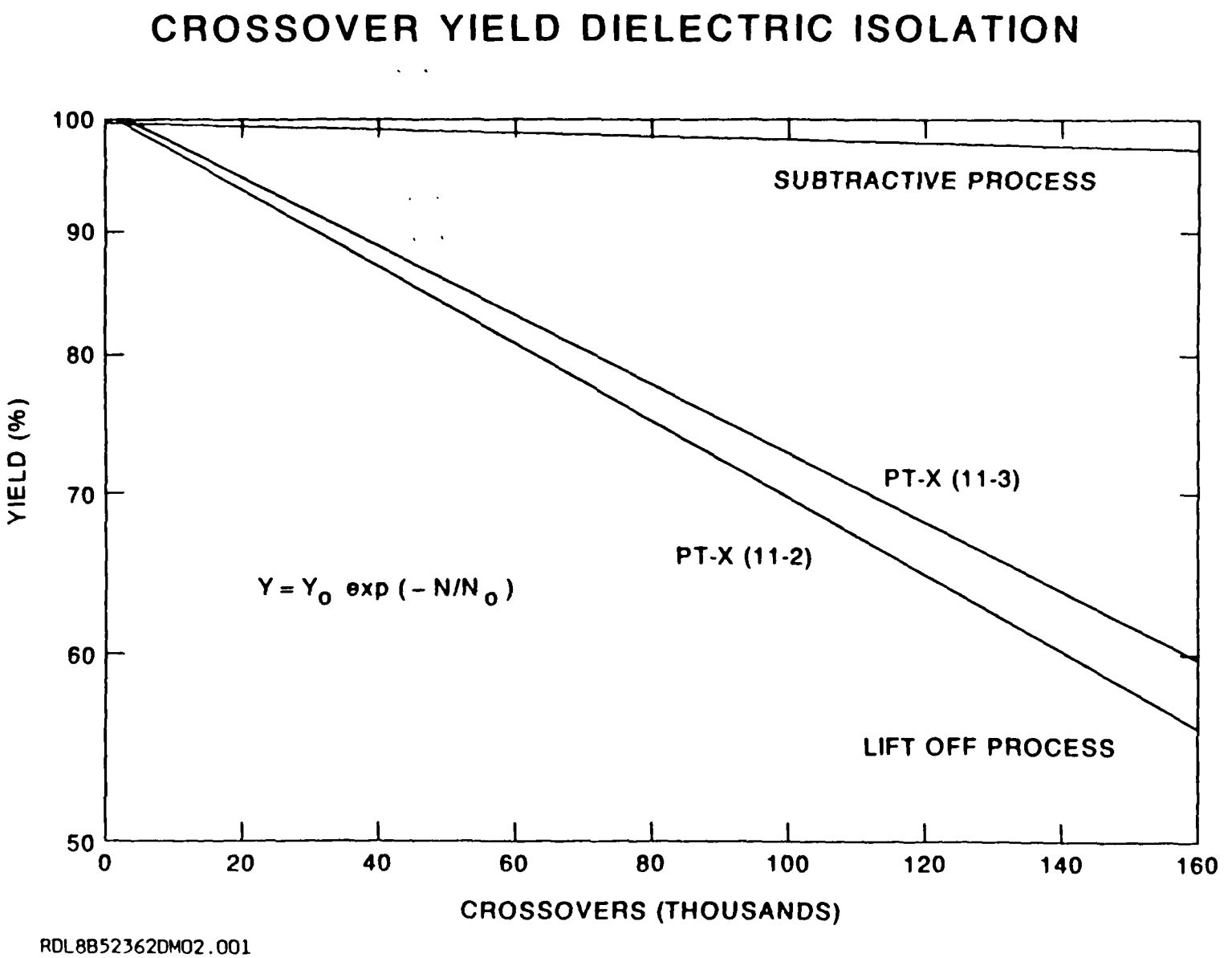


Figure 17. PT-X Crossover Yield for Subtractive and Lift-off Processes

Analysis of split bridge cross test results show that WSi gate lengths of less than .5μm can be uniformly fabricated across a wafer. (Table below.) Target gate lengths in PT-X for the WSi and the Ti/Pt/Au metals are 0.5 and 1.0μm respectively.) Variations in the gate length from lot to lot is attributed to process changes made in lithography studies. Gate lengths of 1μm are reproducible using metals that must be lifted off. The larger variation in the pitch shows slightly less control than for the plasma etched WSi.

PT-X LINEWIDTHS

WAFER	WIDTH	SIGMA	PITCH	SIGMA
	μm	μm	μm	μm
W_xSi_{1-x}				
PTX3-2	.40	.01	2.88	.000
PTX3-4	.37	.01	2.88	.000
PTX10-2	.57	.03	2.89	.007
PTX12-1	.47	.03	2.90	.004
PTX12-2	.55	.02	2.90	.006
Ti-Pt-Au				
PTX3-2	.99	.03	2.96	.017
PTX3-4	.97	.03	2.94	.018
PTX10-2	1.09	.04	2.97	.032
PTX12-1	1.14	.04	2.98	.021
PTX12-2	1.09	.03	2.98	.019

3.4 Advanced Technology (R. H. Burton, A. G. Baca, A. I. Faris and K. W. Wyatt)

The goal of the advanced technology program is to increase circuit speeds to 400 MHz with minimum power consumption. An outline of the plan is given in Figure 18. Successful completion of the plan requires a reduction in parasitic delays and device delays, as well as novel circuit design approaches which reduce the number of effective gate delays in a large circuit. The parasitic delays will be addressed by a reduction in design rules from 2.0μm to 1.5μm as well the implementation of a lower dielectric constant film. Implementation of a submicron gate length device will simultaneously allow lowered device delays as well as parasitic delays through compaction afforded by smaller, higher current drive devices. Evaluation of 1μm and submicron SQT devices will be made in order to compare short channel performances for SQT and baseline HFETs.

Circuit simulations will demonstrate which critical delays are more important in determining circuit speed. Process development activity focus will be determined by the outcome of the circuit simulations. Phase I process development activities will include some or all of the following: reduction of design rules, implementation of lower dielectric constant films, submicron gate definition, lightly doped drain structure using sidewalls, rapid thermal annealing, and W/WSi bilayer gates. Phase II process development activities will focus on yield improvement activities. Two design/process iterations are planned. The APT-1 maskset will provide designers empirical data of devices and small circuit elements needed for design of demonstration circuits on APT-2. APT-1 will also be used to evaluate design rules and currently forbidden layout approaches such as layout of top metal over active areas. In addition,

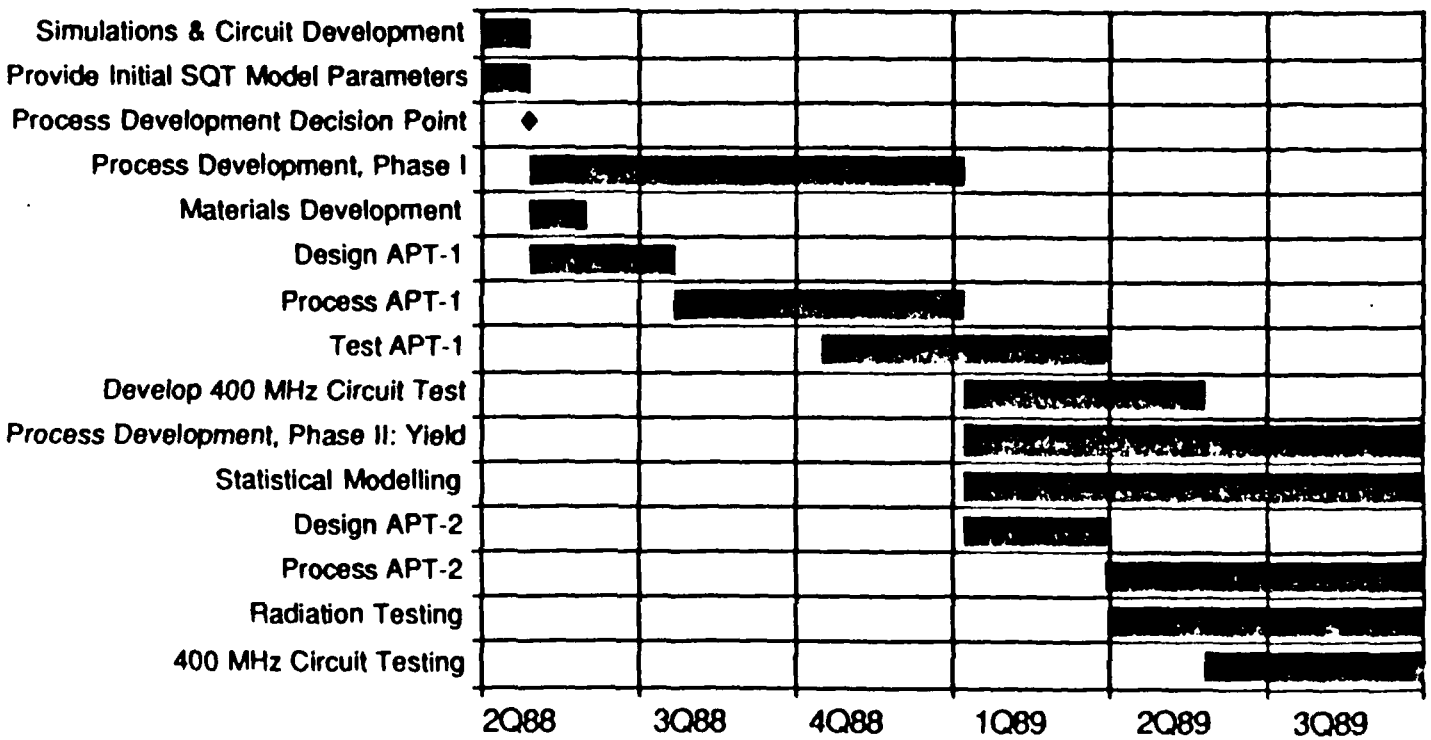


Figure 18. Advanced Technology Development Plan.

APT-1 will include test structures for modeling. A statistical model will be provided at the end of the program in order to allow sufficient time to extract meaningful best and worst case parameters. Design for APT-2 will focus on layout and circuit design approaches which will compact the circuit and reduce the number of required gate delays. Also included in the plan are 400 MHz and radiation testing programs.

The advanced technology program will establish the feasibility of a technology that will achieve 400 MHz speeds with minimal power increase over the baseline technology. Feasibility will be demonstrated for achieving the 3% yield by month 42. Models and design rules will be available in anticipation of Option II redesign of Pilot Line III circuits as well as for outside users wishing to design into the foundry.

3.5 Device Packaging (K. J. Brady)

PT-1, PT-2 (Memory), 4K SRAM

The 24 signal/44 total I/O leaded ceramic flatpack from TriQuint was selected to package these chips. This is a true high speed package, designed with 50Ω signal lines and provision for mounting bypass capacitors on the package. Tests on the commercial high frequency test fixture have shown this package to be good to 1 GHZ. The package has a high thermal conductivity die attach substrate, and it can be hermetically sealed.

Three of these packages were subjected to 200 cycles of -65 to 150°C thermal cycling per MIL STD 883C, Method 1010.7 Condition C. No evidence of damage was found. A sample of fifteen leads were pull tested per MIL STD 883C, Method 2004.4, Test Condition A. No evidence of damage was found. The samples for a full package qualification test per an AT&T document are being assembled.

A total of 500 packages, 50 burn-in sockets and 20 high frequency test fixtures have been received. A trim-and-form tool to bend the leads for a chip face up surface mounting has been ordered. This tool should arrive by May 1, 1988. The current plan is that we will use this package for the PT-2 memory chips and the 4K SRAM.

PT-2 (Logic)

The 64 signal/88 total I/O leaded ceramic flatpack from Interamics (Mayo design) was selected to package these chips. Again, this is a true high frequency package with 50Ω signal lines, some built-in bypass capacitance, and a high thermal conductivity die attach substrate. It can be hermetically sealed.

One hundred of the packages have been ordered. Delivery is promised for 7/1/88. Quotes have been received for the low frequency carriers/sockets; the tooling cost is $60K, and delivery is 18 weeks. The decision to order these parts has not been made. The high frequency test fixture is being developed in-house.

Casino Test Chip

Preliminary electrical analysis indicates that the best available package for this chip is the 256 I/O fine pitch leaded chip carrier designed by AT&T for the EMSP project. Although it is the best available, this package is not ideal for this application. It has a ground plane, but its configuration will probably limit circuit performance to below 200 MHz. The cavity size is

much bigger than the Casino Test Chip, so parasitics due to long bond wires will be present. Like other high pin count packages, it does not have a high thermal conductivity die attach substrate.

The packages are available, and the carriers/sockets will be available in May. A modification of this package to bring it to a true high frequency package is under consideration by in Department 52124.

3.6 Availability of Foundry Mode Chip Fab (D. P. Chabinec, D. A. Harrison, K. W. Wyatt)

In keeping with the Statement of Work, Pilot Line III is now ready to process one lot per month using masks provided by the government or its contractors. Wafers and devices from these lots will be tested for functionality provided test vectors are also supplied (by the customer), compatible with the Advantest T-3340. Non-return-to-zero format test vectors (compatible with a VAX-VMS or UNIX operating system) on magnetic tape is required. The upper limit frequency for functional testing is 160 Mbits/s at 128 pins, maximum. Alternatively, functional testing can be performed at 80 Mbits/s at 256 pins, maximum. Twenty of the most promising chips will be packaged, and the remainder will be delivered as chips or marked wafers.

For customers who prefer to use a full custom approach, design rules and AT&T's exclusive ADVICE circuit simulation software will be available on April 1, 1988, allowing the customer to do his own design and simulation (see attached Design Rules). AT&T will also accept designs on magnetic tape in the GDS II format for mask generation. As an alternative, AT&T will also accept logic diagrams or a functional concept and provide design, simulation, layout, and manufacturing services.

Initially, for customers wishing to use standard cells, AT&T will provide design, simulation, layout, and manufacturing services. In September of 1988, a design manual and a standard cell library will be available. This in combination with AT&T's ADVICE simulation software will allow the customer using standard cells the option of doing his own design and simulation. AT&T will do the layout and manufacturing.

For wafers processed in the foundry mode, all manufacturing will be done in the 10,000 square foot Class 1 clean room located at AT&T in Reading, Pennsylvania. Devices will be fabricated in the planar SARGIC/HFET (Self Aligned Refractory-Gate Integrated Circuit Heterostructure FET) process that is based on a 1 micron gate length. Devices available in this process include Enhancement and Depletion mode HFETs, Schottky Diodes, N+ ion implanted resistor, and Metal-Insulator-Metal Capacitors. Two level metal inter-connection with 2 micron line width and spacing is available. Device isolation is achieved by an oxygen implant between active regions. This process is well suited to the development of custom LSI circuits. Complexities to 3500 equivalent gates have been designed for the Pilot Line III program. The 1 micron gate SARGIC process DFET and EFET f_T's exceed 18 GHz.

To access this foundry or for additional information, please contact David Harrison at (215) 939-6457 or Edward Letchak at (215) 939-3242.

4. Radiation Hardness, Reliability, and Quality

4.1 Radiation Hardness Testing (S. B. Witmer, S. D. F. Jones, R. L. Remke)

Transient Radiation Testing

PT-0 AlGaAs/GaAs heterostructure FETs (HFETs) were irradiated with 20nsec pulses of 40MeV electrons at the Naval Research Laboratory in Washington, DC. Positive voltage transients were measured at the drain node and negative voltage transients were measured at the gate node of the HFETs during the irradiation (Figure 19). These results indicate that the photocurrent flows into the gate and out the source and drain. The magnitude of the transient voltages strongly increased with dose rate. The transient gate and drain currents are reduced slightly with decreasing gate voltage and increasing drain voltage. The transient voltages observed during irradiation are believed to result from the collection of electron-hole pairs within the depletion regions of the junctions (photovoltaic effect). The photocurrent generated in the heterojunction depletion region dominates over the photocurrent generated in the Schottky barrier depletion region and hence the observed result of current flow into the gate of the HFET. The substrate currents, which dominated earlier measurements, were reduced by growing a silicon nitride layer under the metallization and by growing a superlattice structure in the GaAs. The reduction in substrate current made it possible to characterize the photovoltaic effect.

Total Dose Testing

Total dose radiation testing was performed on PT-0 HFETs and ring oscillators. The DC characteristics were measured before and after exposure to $1x10^8$ rad(GaAs) of gamma radiation from a Co^{60} source. The HFETs were tested with and without bias. After $1x10^8$ rad(GaAs), no measurable change in the DC characteristics was observed for biased or unbiased HFETs. Figure 20 shows the drain current both before and after irradiation with 0.7V gate bias.

Ring oscillator AC characteristics were measured before and after irradiation. After $1x10^8$ rad(GaAs), the average drain bias current decreased by 6.8% and the frequency decreased by 4.2%,

Single Event Upset Testing

Single event upset testing was performed on PT-0 HFETs. Alpha particles emitted from 1μ Ci of Am^{241} were used to irradiate the HFETs. Negative voltage transients were measured at the drain node during the alpha particle irradiation using the experimental setup shown in Figure 21. The transient response for HFETs was much smaller than that observed for MESFETs as shown in Figure 22. This result suggests that memories made with HFETs will be more immune to single event upset than those made with MESFETs.

4.2 Reliability (Y. L. Cho, R. L. Remke)

Reliability efforts during the reporting period were directed to REM (reliability evaluation module) aging/testing including electromigration experiments for the Ti/Pt/Au metallization system. The electromigration experiments were performed on PT-0 REM top metallization strip patterns, as shown in Figure 23. The samples were subjected to different sets of stress levels to induce failures which in turn would enable us to determine the activation energy E_a

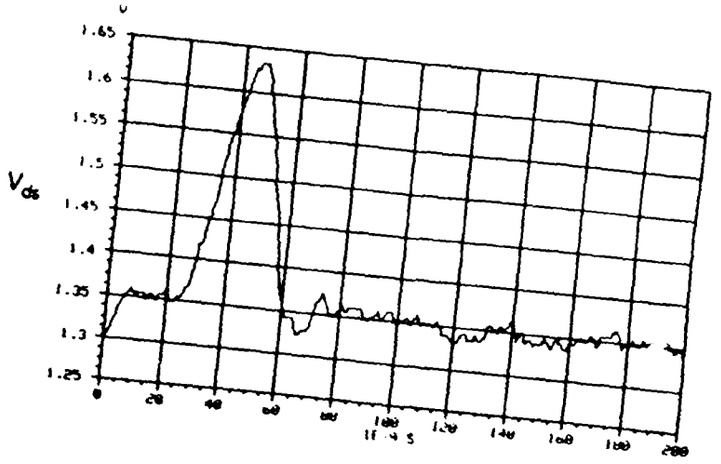


Figure 19a. PT-0 Wafer 3223 FET Drain Voltage (V_{ds}) response to 5×10^{10} rad(GaAs)/s (V_{DD} = 1.5 V, V_{GG} = 0.6V)

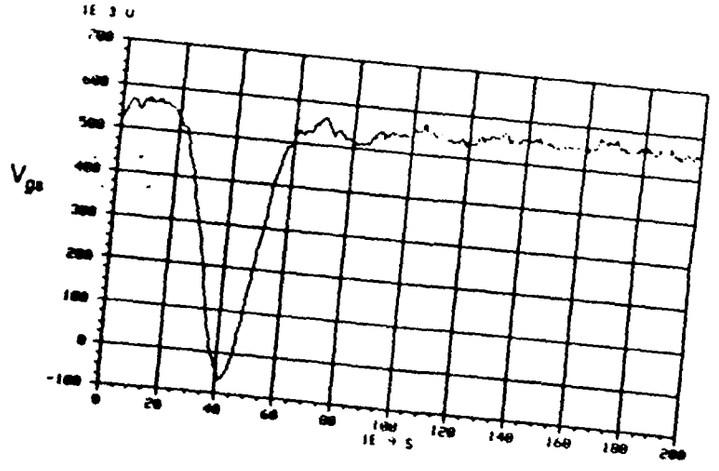


Figure 19b. PT-0 Wafer 3223 FET Gate Voltage (V_{gs}) response to 5×10^{10} rad(GaAs)/s (V_{DD} = 1.5 V, V_{GG} = 0.6V)

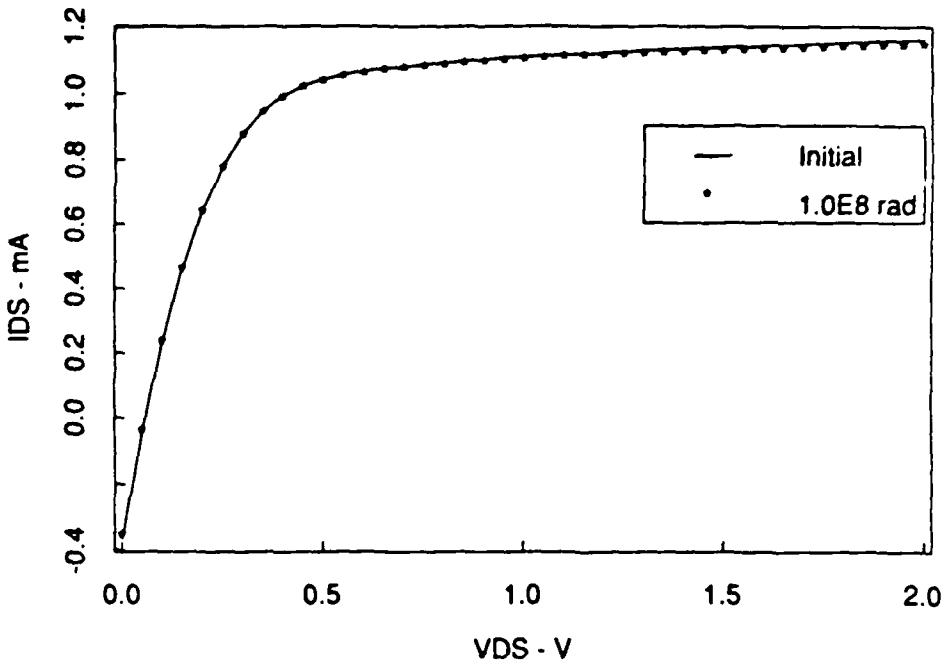


Figure 20. PT-0 Wafer 3223 FET Drain Characteristics as a Function of Total Ionizing Dose. (Biased, V_G = 0.7 V)

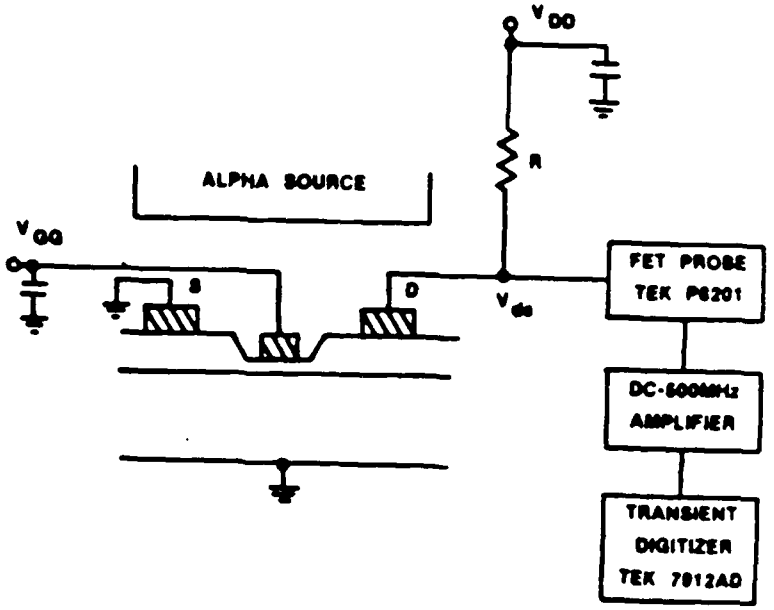


Figure 21. Experimental Setup for Alpha Particle Irradiation Experiments.

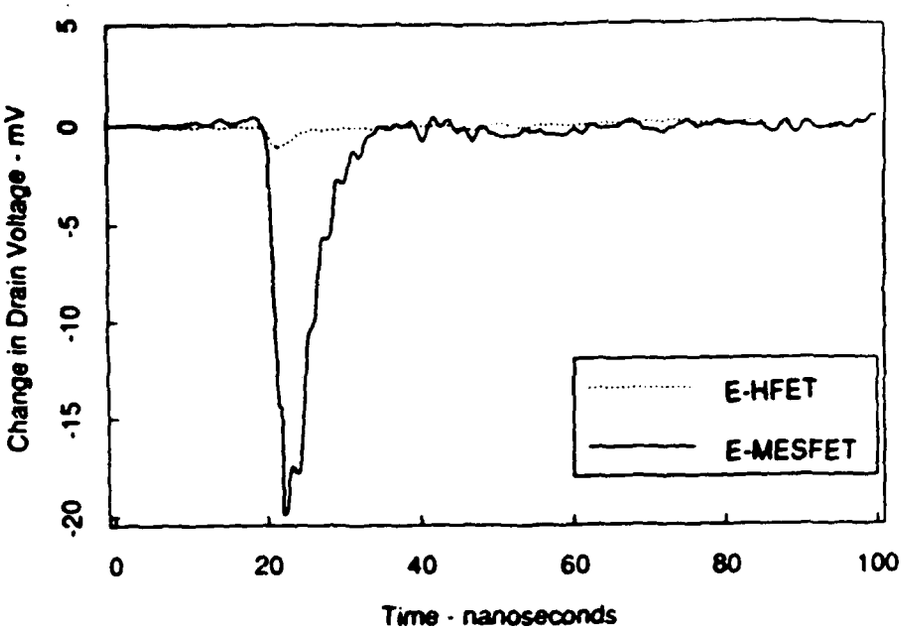


Figure 22. The Drain Voltage Response of an E-MESFET and an E-HFET to an Alpha Particle. V_{GG} = -0.5 V, V_{DD} = 1.5 V, Gate Length = 1.0 μm, Gate Width = 17.5 μm.

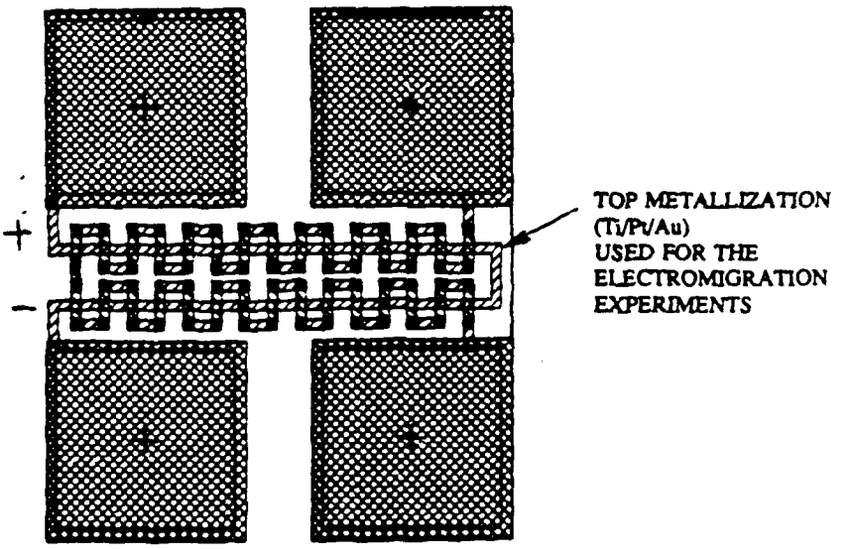


Figure 23. PT-0 Electromigration/Dielectric Test Pattern.

and the n-factor from Black's expression (J. R. Black, "Electromigration - A Brief Survey and Some Results," IEEE Trans. Electron Devices, ED-16, April 1969). According to the model, median time to failure (MTF) can be written as:

$$MTF = AJ^{-n} \exp [E_a/k_B T]$$

where A=constant, J=current density, k_B=Boltzman's constant, and T=temperature in degrees Kelvin.

At the high stress level of 250°C and current density of $J = 7 \times 10^6$ A/cm^2, we have been able to induce an electromigration failure on the Ti/Pt/Au metallization in a relatively short period of time. During this aging, the resistance of the metallization increased steadily up to 70th hour (Figure 24). At this point, the resistance started to fluctuate. A microscopic inspection showed a series of void formations in the metallization line, and the resulting mass transport was clearly observable (Figure 25).

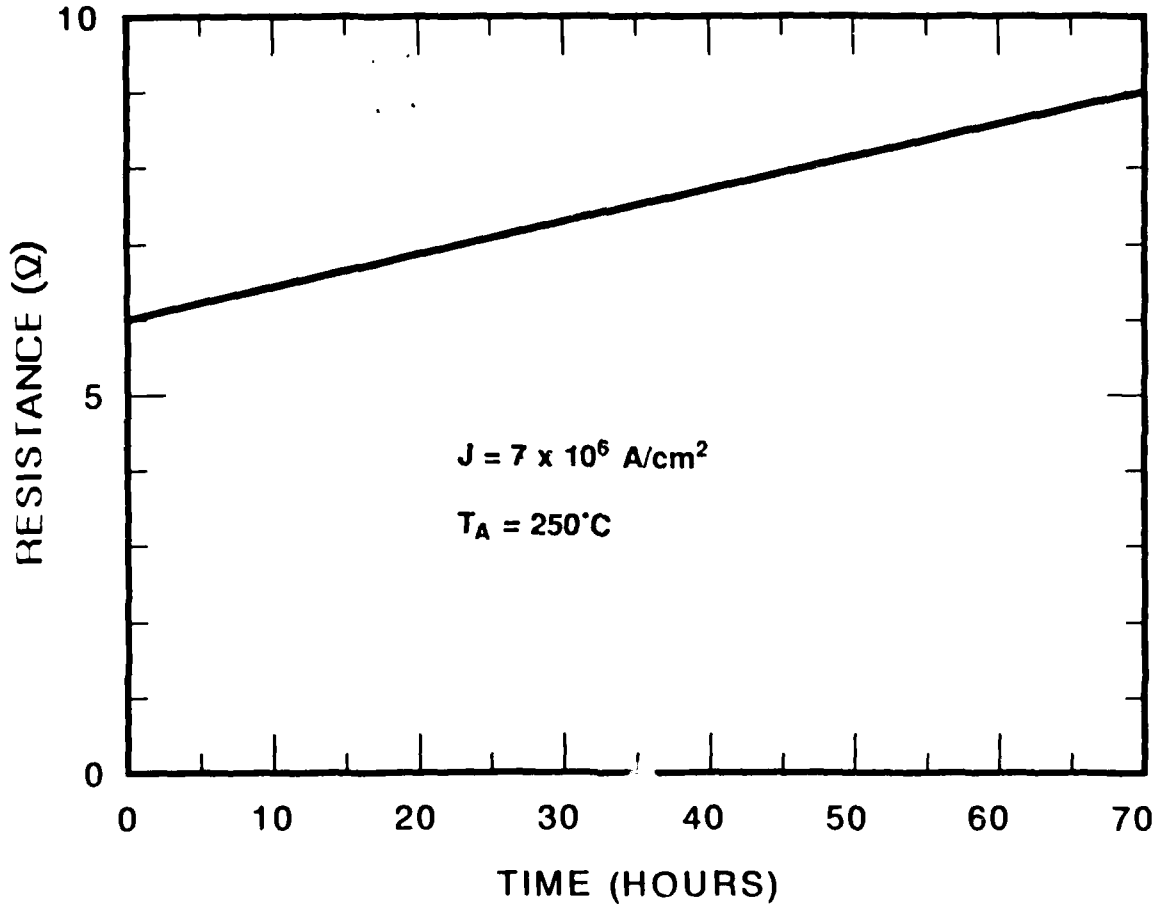
We also performed a 1,000 hour aging test where the stress level was considerably lower (T_A = 200°C, $J = 1 \times 10^6$ A/cm^2). As a result, the resistance variation during the entire aging period was less than 3% (Figure 26). Using the failure criteria of 10% change in resistance, an extrapolation leads to a time to failure (TTF) of approximately 3×10^6 hours at the stress level. The TTF at use conditions is therefore expected to be considerably longer. In the next reporting period, the actual failure rate will be established from an appropriate statistical modeling.

4.3 Quality Program, AT&T (R. D. Frantz)

The quality program for Pilot Line III has progressed in step with process development. Process control measurements have been instituted throughout the line and control charts have been established wherever they are useful. Presently there are 16 process control measurements being used in the MBE growth process and 45 measurements being used in the wafer fabrication part of the Pilot Line. Shop measurement standards are being maintained through the use of control charts, and the performance of the clean room environment is being monitored and charted. All but a few of these process controls are being performed by the shop, and most of the data are being entered into the QUEST data base for automatic updating. In the test and characterization area, a UNIX based system better suited to the present work is being used to process data and generate control charts. At this time, 48 different charts are being used by engineering for device characterization.

The Shop Flow System, a computerized system for controlling the flow of material through the production line, has been fully implemented in the wafer fabrication portion of the pilot line, and is being implemented in the MBE area. This system is used to keep track of wafer lots. It stores and reports lot locations, yields, time at each operation, operator identification, rework, etc. The system also contains operator instructions and accepts process control data that are automatically transferred to the QUEST System to update control charts.

Documentation of the process is complete from the beginning of the process through wafer fabrication. Drawings and process instructions have been created by Bell Laboratories. From these engineering documents, AT&T Microelectronics Shop Instructions have been written. Although there will be further changes to the process as it develops, the changes will be controlled and documented by the change control procedure. Documentation of the packaging process is in place for PT-1 prototypes and can be adapted to future needs.



RDL8B52365SN01.002

Figure 24. Resistance as a Function of Time for PT-0 Electromigration Tester.

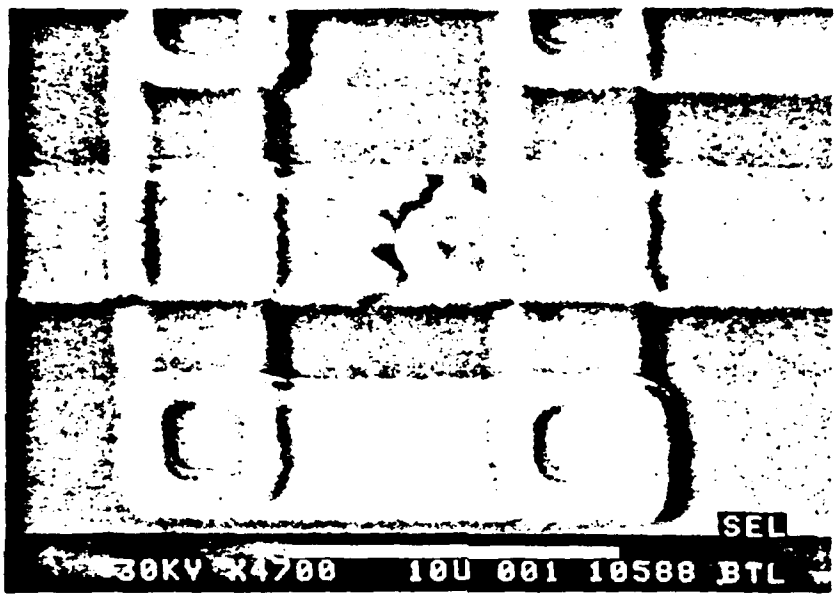
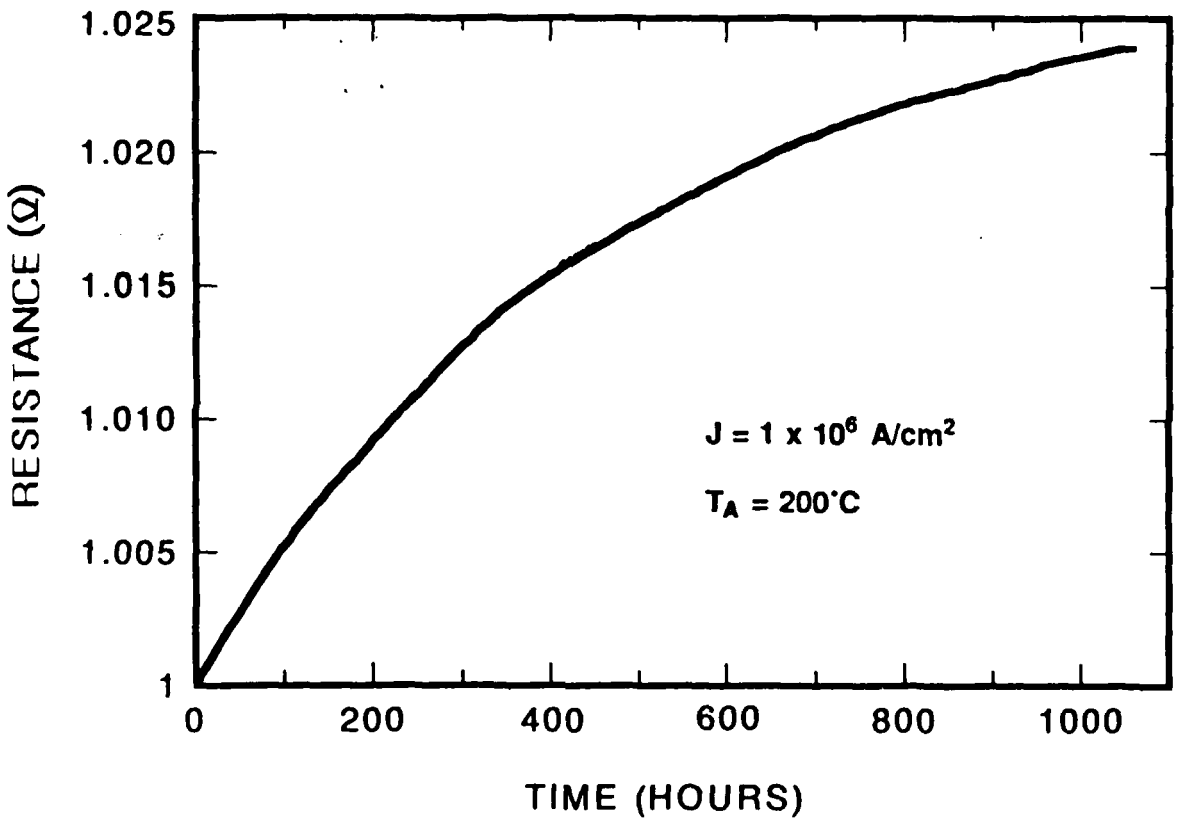


Figure 25. Metal Migration Voids Formed due to Current and Temperature Stressing.



RDL8B52365SN01.001

Figure 26. Normalized Resistance as a Function of Aging Time.
An Extrapolation Predicts a Time to Failure of more than 3 x 10^6 Hours.

4.4 Quality Control Procedures at Hughes (R. N. Sato)

On March 8 and 9, 1988, a meeting was held at Torrance, California, to discuss the Hughes Microwave Products Division (MPD) Quality program with personnel of the AT&T Quality Planning Department to Reading, Pennsylvania. The participants included R. D. Frantz and M. J. Hoffman of AT&T and P. J. Nobile, the MPD Quality Manager. The major objective was to insure that the MPD quality program will meet the DARPA contract requirements.

Quality procedures and documentation currently in place at MPD were reviewed in detail. The scope and content of the MPD quality manual, which defines the overall quality program, are similar to the corresponding AT&T document. The current production control system and incoming inspection and vendor quality systems were also reviewed. MPD is currently upgrading its production control system to a system similar to AT&T's Shop Flow.

A tour of the MPD GaAs IC production facility focused on recently installed production processing equipment. Currently, a major effort in automated in-process testing and data analysis is being directed to the establishment of statistical control in the process line.

In general, it was concluded that the MPD quality system can meet the requirements of the Pilot Line III program.

APPENDIX A

Pilot Line Facilities and Process Control

(J. H. Duchynski, V. N. Patel)

The 3" VLSI GaAs IC pilot line has been established with an initial capacity to process up to 33 SARGIC HFET wafers/week including in-process testing for PCM's that will be used in the foundry (see attached Design Rules). In addition, the line has capacity to process up to 67 non-MBE wafers/week bringing the total initial line capacity to 100 wafers/week (five days, 3 shift basis). Wafer probe, packaging, and final device testing will be scaled according to the needs of the specific customers, complying with the foundry requirements outlined in Section 3.6. The foundry will circuit test lots fabricated with Government-supplied reticles if the test vectors are compatible with our test sets.

Clean Room

Construction of the 3" GaAs IC clean room was completed and certified to comply with Class 1 FED STD 209. Clean room environment is monitored routinely and plotted on control charts. The results indicate that the room maintains the cleanliness level required for fabricating high yield VLSI circuits. Routine monitoring of particle count for particle size of 0.2uM and 0.5uM shows that the room does not exceed the Class 1 limit of four and three particles per cubic foot respectively, and on the average is well below two particles per cubic foot.

Operating Staff

The line is staffed with 21 operators. Operators are being added on the second shift in the MBE, testing, and photoresist areas to shorten process interval. Training is continuing to improve skills required to make SARGIC HFET a production process.

Facilities

Table A1 indicates the dates on which some of the key silicon-like high volume manufacturing equipment were ready to commence development of the 3" SARGIC-SDHT process. Prior to installation, the equipment was thoroughly cleaned, and at completion of installation and prove-in, reports were generated reflecting that the equipment was ready for process development. The reports are available on request from our files.

Facilities Management

Uptime of each of the facilities in the clean room is monitored with automatic logging of preventive and routine maintenance history kept on the FACMAN (AT&T's computerized Facilities Management System).

Line Management

Shop Flow reports on all starts, processing interval, yields and inventory by operation are generated daily and available for line management. The Shop Flow is a corporate wide computerized line management system.

Shop Instructions

Shop instructions and processing instructions are in place. Table A2 summarizes the list of all shop instructions. Processing instructions held in Shop Flow are almost complete.

Manufacturing

All processing operations are performed in the Pilot Line with the exception of Ohmic evaporation, Ohmic alloy, implant anneal, passivation etch and via etch. Other than via etch, all the operations are performed in other clean rooms. Via etch operation will be transferred to the Pilot Line in 3Q88.

Process Controls

Process control charts were created for all critical parameters. A current list of the process control charts in the line is attached in Table A3. All charts are updated on a regular frequency based on line volume, lot size, and control parameter. Other control charts are planned to be incorporated during the next quarter.

TABLE A1

PROCESS OPERATION	EQUIPMENT	EQUIPMENT PROVE-IN DATE
MBE GROWTH		
Epitaxy	MBE GENII #1	April 1987
	MBE GENII E#2	February 1988
Outgassing	Varian Outgas System	October 1987
Post Epi inspection	Hall Test Set	September 1987
Acid/Solvent sink	Santa Clara	February 1987
Contrast Int. Microscope		July 1987
LOT START		
Inspect Wafers	Tencor 4500	June 1987
Wafer Flatness	Tropel Autosort	February 1987
Wafer Identifier	APT 280AN	April 188
PHOTOLITHOGRAPHY		
Expose Tools	Nikon 1505G4C	May 1987
Scrub/Bake/Apply Track	Eaton 6000	July 1987
Develop/Bake/Apply Track	Eaton 6000	July 1987
Linewidth Measurement	SEM	November 1987
PR Descum	Tegal 515	October 1987
PR Strip	Tegal 915	July 1987
Litho Adviser	Promatrix	May 1987
Flood Expose	HTG	October 1987
IMPLANT & ACTIVATE		
Ion Implant	Varian 350D	June 1987
Implant Activate	AG RTA 2101	September 1987
Implant Dose Monitor	P.I. Isoscan 2	May 1987
METAL DEPOSIT		
Gate Metal - WSi	MRC 943	June 1987
Ohmic Deposition	Temescal	August 1987
Final Metal	Temescal	May 1988
Final/Int. Conn. Metal	MRC 943	October 1987

TABLE A1

PROCESS OPERATION	EQUIPMENT	EQUIPMENT PROVE-IN DATE
METAL PATTERN TRANSFER		
Gate Metal Etch	AMT 8120	June 1987
Lift Off Station	MTI	October 1987
DIELECTRIC DEPOSITION		
Silicon Oxide	Electrotech 6200	Januay 1988
DIELECTRIC ETCH		
Silicon Oxide	AMT 8120	December 1987
Silicon Nitride	Tegal 901E	December 1987
WET CHEMISTRY		
Wafer Etch/Clean	APT 9165	September 1987
Cap Strip/Clean	FSI Zeus	June 1987
Megasonics	2000AT	September 1987
Rinser/Dryers	Semitool	June 1987
Etch/Clean Sinks	Santa Clara	June 1987
Acid Mixing Sink	Santa Clara	June 1987
TESTING		
PCM Tests	HP 40628	November 1987

TABLE A2

PROCESS OPERATION	EQUIPMENT	SI #	ISSUE #
LOT START			
Incoming Waf. Insp.	Surfscan 4500	88RD0150	Issue 1
Wafer Prepartion	Acid/Solvent Sink	88RD0160	Issue 1
Wafer Load	MBE GEN II	88RD0170	Issue 1
Trolley Load	MBE GEN II	88RD0180	Issue 1
MBE Growth	MBE GEN II	88RD0190	Issue 1
Defect Counting	Microscope		
	Surfscan 4500	88RD0200	Issue 1
Mobility Test	Hall Test Set	88RD0210	Issue 1
Control Charts		88RD0059	Issue 1
Wafer Flatness	Tropel Autosort	planned	Issue 1
PHOTOLITHOGRAPHY			
Expose Tools	Nikon 1505G4C	88RD0069	Issue 1
Scrub/Bake	Eaton 6000	88RD0012	Issue 1
Apply/Bake	Eaton 6000	88RD0013	Issue 1
Develop/Bake	Eaton 6000	88RD0014	Issue 1
PR Coat/Bake	SVG Tracks	88RD0034	Issue 1
Visual Inspection	Microscopes	88RD0050	Issue 1
Apply - Sink	Sink	88RD0055	Issue 1
PR Bake	Ovens	88RD0051	Issue 1
Photomask Cleaner		88RD0052	Issue 1
Photomask clean - sink	Sink	88RD0054	Issue 1
Linewidth Measurement	Leitz MPV-CD	88RD0053	Issue 1
Contact Aligners	Cannon	88RD0049	Issue 1
Alpha Step 200	Alpha Step	86RD0254	Issue 2
Vapor Prime	Yield LP3	88RD0015	Issue 1
PR Thickness Measurement	Nanospec	88RD0016	Issue 1
PR Strip	Tegal 915	88RD0017	Issue 1
Manual Develop Sink		88RD0018	Issue 1
PR Descum	Tegal 515	88RD0019	Issue 1
Wafer Identifier	APT 280AN	NEW	Issue 1
IMPLANT & ACTIVATE			
Ion Implant	Varian 350D	87RD0001	Issue 1
Implant Activate	Furnace Anneal	88RD0020	Issue 1
METAL DEPOSIT			
Sputter Metals	MRC 943	88RD0075	Issue 1

TABLE A2

PROCESS OPERATION	EQUIPMENT	SI #	ISSUE #
Evaporate Metals	Temescal	88RD0076	Issue 1
METAL PATTERN TRANSFER			
Gate Metal Etch -WSi	AMT 8120	88RD0071	Issue 1
Lift Off Station	MTI Omnichuck	88RD0077	Issue 1
DIELECTRIC DEPOSITION			
Silicon Oxide	Electrotech 6200	88RD0073	Issue 1
Measure Thickness	Ellipsometer	88RD0074	Issue 1
DIELECTRIC ETCH			
Silicon Oxide	AMT 8120	planned	Issue 1
Silicon Nitride Passivation	Technics IIA	88RD0074	Issue 1
WET CHEMISTRY			
Clean Monitor	Surfscan 4500	88RD0061	Issue 1
Cap Strip/Clean	FSI Zeus	NEW	Issue 1
Megasonic Clean	Megasonics	88RD0008	Issue 1
Etch Sink -EFET	Santa Clara	88RD0006	Issue 1
GaAs Wafer Etch	APT 914 W Etcher	88RD0039	Issue 1
GaAs Wafer Etcher	APT 9165	88RD0038	Issue 1
Future Etches	Manual Etch Sink	88RD0056	Issue 1
PP Etch	APT 9165	88RD0039	Issue 1
			Issue 1
TESTING			Issue 1
Ohmic Tests	HP 4062B	88RD0070	Issue 1
PCM Tests	HP 4062B	88RD0070	Issue 1
OTHERS			
Control Charts		88RD0059	Issue 1
Process Check Instruc.		88RD0011	Issue 1
			Issue 1

TABLE A3

CHART #	OPERATION	PARAMETER	FREQUENCY	SAMPLE SIZE	TYPE OF CHART
MBE GROWTH					
P120051	Wafer Inspection	Def./Sq. Cm.	each wafer	1 Rdg./Wafer	U
P120051	Wafer Inspection	300K Mobility	1 per lot	1 Rdg./Wafer	MR
P120051	Wafer Inspection	300K Sheet Den.	1 per lot	1 Rdg./Wafer	MR
P120061	Wafer Inspection	77K Mobility	1 per lot	1 Rdg./Wafer	MR
P120061	Wafer Inspection	77K Sheet Den.	1 per lot	1 Rdg./Wafer	MR
P120071	Wafer Inspection	300K Sheet Res.	1 per lot	1 Rdg./Wafer	MR
P120081	MBE Cal.	22% Al Conc.	1/week	1 Rdg./Wafer	MR
P120081	MBE Cal.	22% Dep Rate	1/week	1 Rdg./Wafer	MR
P120091	MBE Cal.	50% Al Conc.	1/week	1 Rdg./Wafer	MR
P120091	MBE Cal.	50% Dep Rate	1/week	1 Rdg./Wafer	MR
PHOTOLITHOGRAPHY					
W180003	Gate PR	Linewidth	2 Waf/lot	3 Rdgs./Wafer	$\bar{X}$,R
W110002	Gate L.W. Proc. Bias	Promatrix	1 Dummy/Week	22 Rdgs./Wafer	$\bar{X}$,S
W130001	PR Thickness	17,500A	2 Dummy/Day	5 Rdgs./Wafer	$\bar{X}$,R
W180001	PR Thickness	7,050A	2 Dummy/Day	5 Rdgs./Wafer	$\bar{X}$,R
W230001	PR Thickness	12,250A	2 Dummy/Day	5 Rdgs./Wafer	$\bar{X}$,R
W270001	PR Thickness	9,050A	2 Dummy/Day	5 Rdgs./Wafer	$\bar{X}$,R
FET ETCH					
W800001	E FET Etch	Etch Stop Depth	Each Wafer	3 Rdgs./Wafer	$\bar{X}$,R
W800002	Pre-Gate Etch	EFET-DFET Step	Each Wafer	3 Rdgs./Wafer	$\bar{X}$,R
DIELECTRICS					
W190001	Gate Etch	Film Etch Rate	Each Run	1 Rdg./Dummy	M,R
W190002	Gate Etch	PR Etch Rate	Each Run	1 Rdg./Dummy	M,R
W260001	Via Deposit	SiN Thickness	Each Run	5 Rdg./Dummy	$\bar{X}$,R
W280001	Via Etch	Film. Etch Rate	Each Run	1 Rdg./Dummy	M,R
W305001	Pass Dep.	SiN Thickness	Each Run	5 Rdgs/Wafer	$\bar{X}$,R
W310001	Pass Etch	Film Etch Rate	Each Run	1 Rdg./Wafer	MR
W210002	Dielectric Deposit	Stress	Every 10 Runs	1 Rdg./Dummy	MR
W210001	Dielectric Deposit	Thickness	Every 5 Runs	1 Rdg./Dummy	MR
W210001	Dielectric Deposit	Refractive Index	Every 5 Runs	1 Rdg./Dummy	MR

APPENDIX B

Plan for Increasing Throughput

(J. H. Duchynski, V. N. Patel)

Plan

Throughput for the Pilot Line will be gradually increased by inclusion of SARGIC HFET and non-MBE technologies to reach 100 wafer starts/week by 1Q1990. Figure B1 shows the ramp-up plan which includes the AT&T business demand along with the Pilot Line III starts for the deliverables (shaded portion).

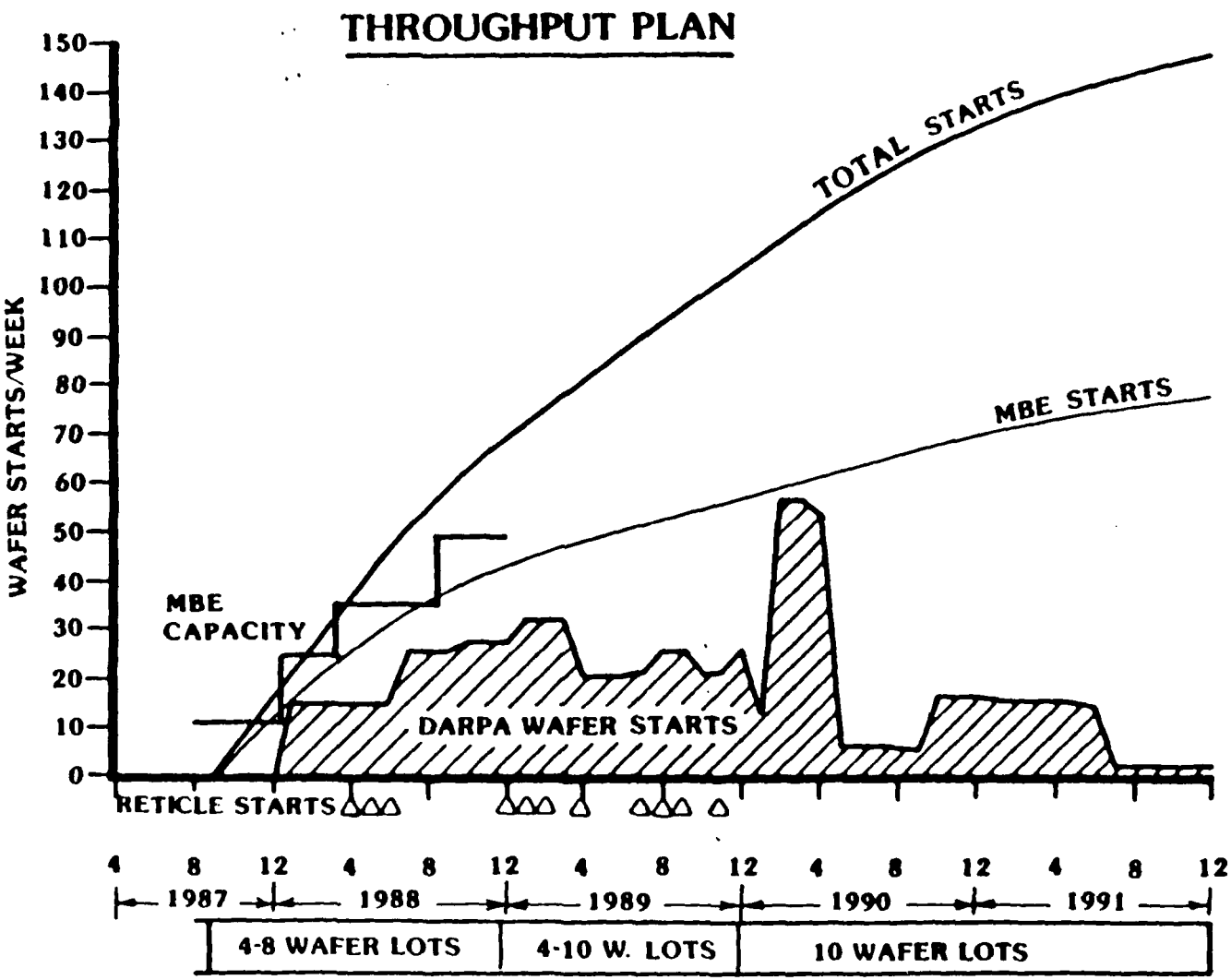
We have averaged 15 wafers/week (Figure B2) with an average lot size of seven wafers/lot in the 1Q1988 for the baseline process development (PT-0) and tester chips (PT-1). The total wafer starts will be increased at a rate which supports the learning curve proposed in our yield plan (Appendix C). The ramp-up plan has shifted out by six months in comparison with the proposal plan, but the overall throughput is essentially the same. The lot size will be increased as Statistical Process Control (SPC) based processing stability is achieved to reach ten wafers/lot by 1Q1989.

Throughput Limitations

The established wafer fabrication line is capable of processing 100 wafers/week on a five-day three-shift basis. The line is currently operated on one-shift basis with skeleton second shift operations in MBE, photoresist, and testing to reduce process development interval. Additional staffing on other shifts will be brought on as the line throughput increases. For the SARGIC HFET technology, the line capacity is limited by the availability of MBE wafers. Figure B3 shows the demonstrated throughput available from the MBE systems. This is projected to reach 46 wafers/week for the DARPA production structures in 4Q1988. The MBE capacity limits are also shown in Figure B1 for comparison with the overall business plan.

Demonstration Vehicles

The schedule for increase in Pilot Line III starts and schedule for reticles is shown in Figure B4. Planned ramp-up for DARPA and AT&T starts to achieve the critical manufacturing discipline, operator awareness and process development for yield improvements are related to timely and orderly development of the demonstration vehicles.



DARPA Pilot Line III and AT&T's Business

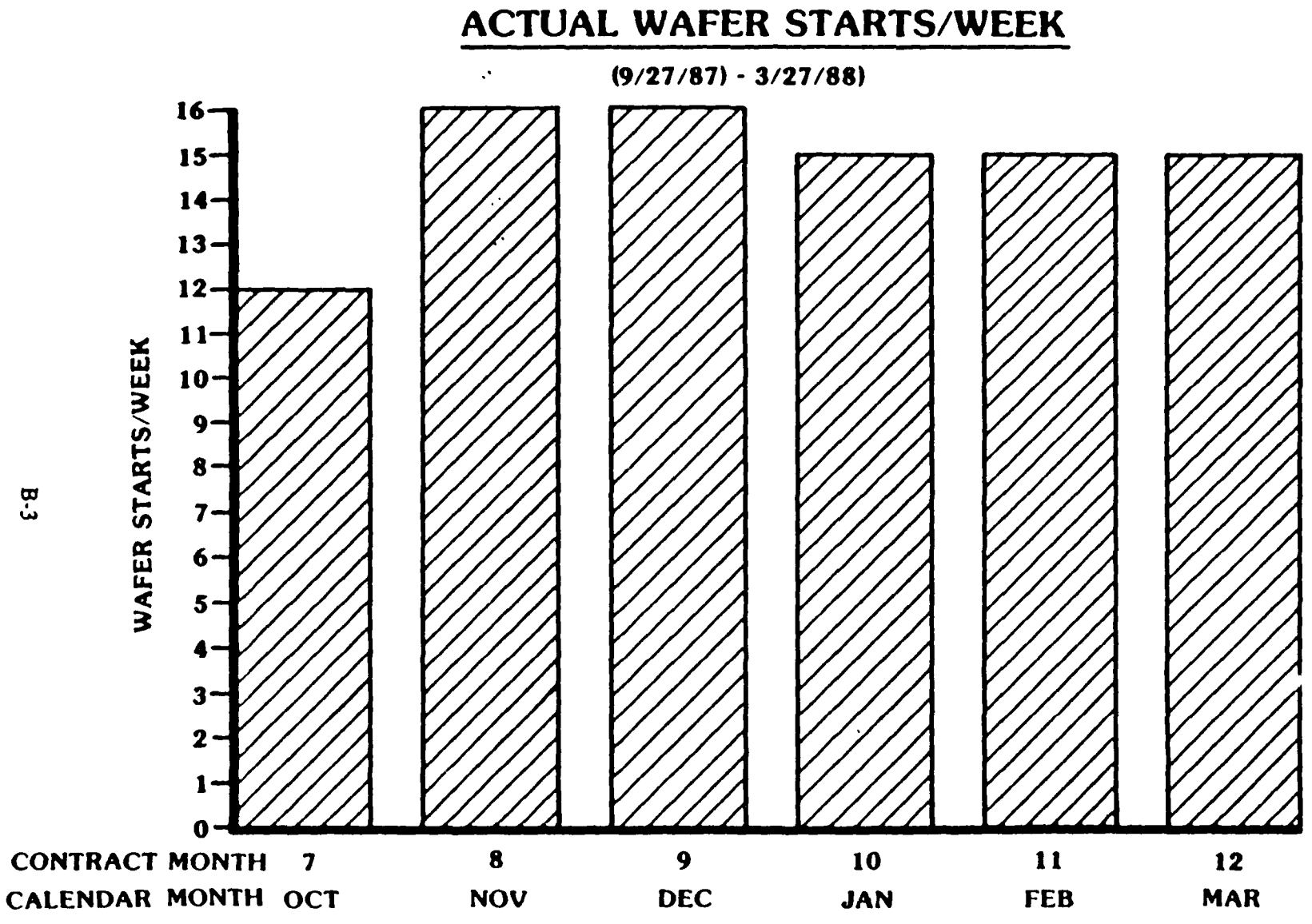
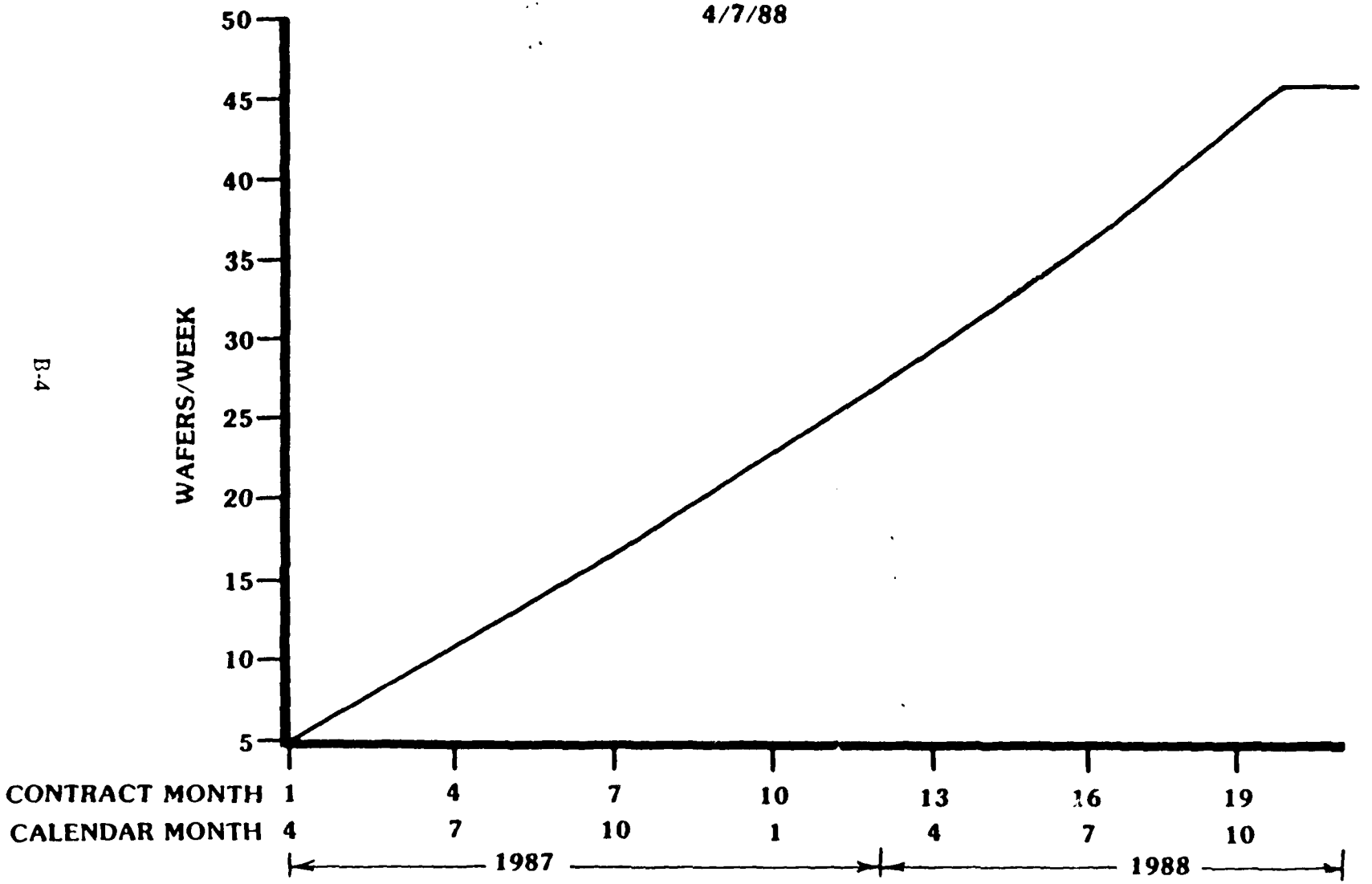


Figure B2. SARGIC HFET Wafer Starts per Week for October, 1987, Through March, 1988.

MBE RAMPUP PLAN

4/7/88



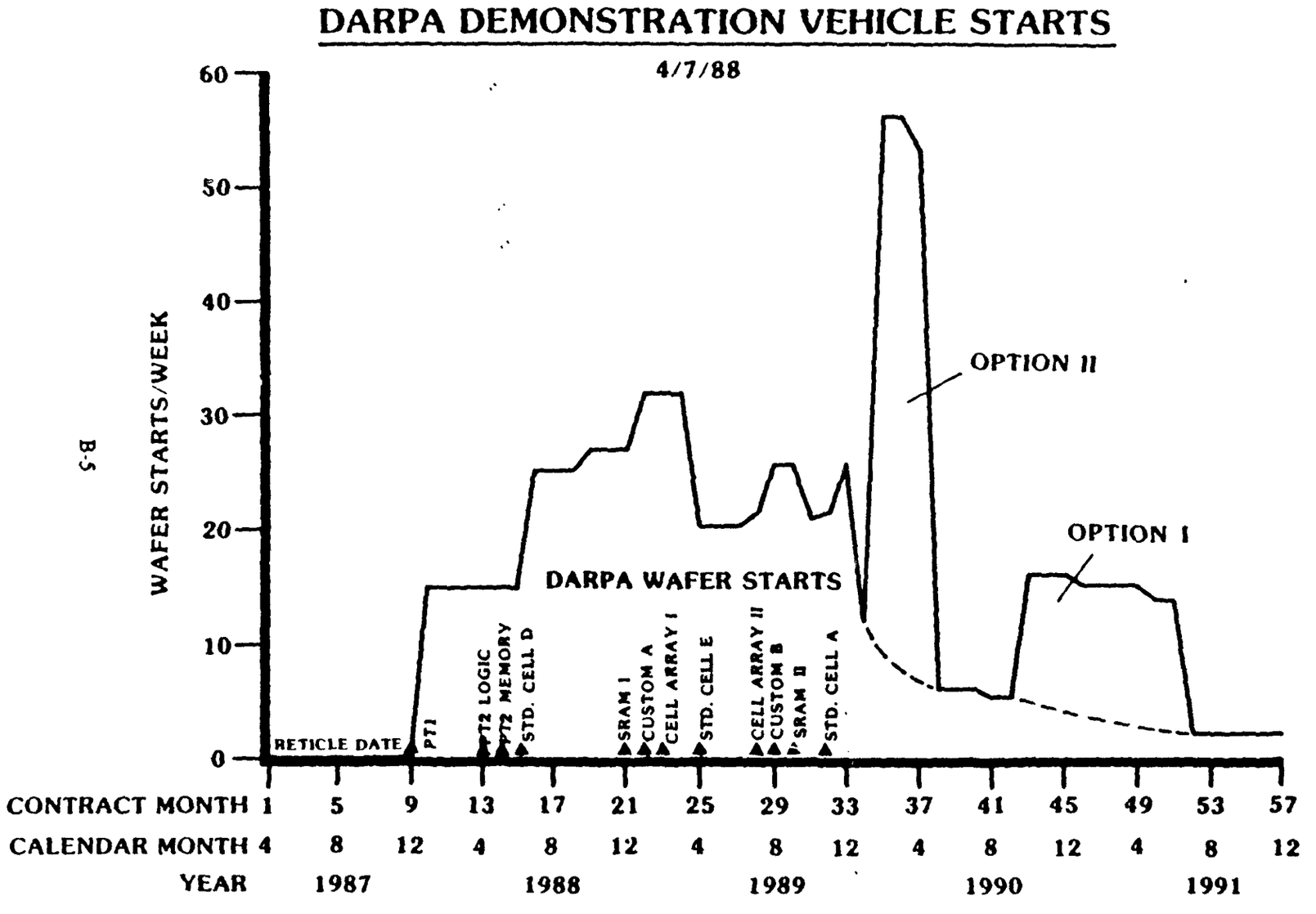


Figure B4. DARPA Pilot Line III Wafer Starts for Demonstration Vehicles.

APPENDIX C

Plan for Evaluation of Yield Trends

(J. H. Duchynski, V. N. Patel)

Introduction

We will achieve the DARPA objective of a 10% DC probe yield by October, 1990, by extending the yield improvement procedures developed in our silicon lines to SARGIC HFET circuits. The rate of yield improvement is linked to a learning curve, and a methodology has been developed to collect and analyze data to identify specific yield improvement tasks. Murphy's yield model (B. T. Murphy, Proc. IEEE (1964), p. 1537) will be validated for GaAs and used in planning and forecasting yields for future DARPA demonstration vehicles. The yield plan will be updated semiannually.

Yield Measurements

The following key yield components will be monitored and analyzed: MBE, wafer throughput, PCM test, DC wafer probe, and final package test. The yield definitions are:

YIELD COMPONENT	DEFINITION
MBE Yield	$\frac{\text{Device Quality MBE Wafers}}{\text{MBE Wafer Starts}}$
Wafer Throughput Yield	$\frac{\text{Wafers Ready for PCM Test}}{\text{Wafers Started in Fab Line}}$
PCM Yield	$\frac{\text{Number of Good PCMs}}{\text{Number of PCMs Tested}}$
DC Wafer Probe Yield	$\frac{\text{DC Functional Sites}}{\text{Number of Sites Tested}}$
Package Test Yield	$\frac{\text{Number of Functional Packages}}{\text{Number of Packages Tested}}$

Learning Curve

The rate of yield improvement is linked closely to the total throughput of the pilot line. The aggressive learning curve for the SARGIC HFET technology (Figure C1) required to attain a 10% DC functional yield for DARPA demonstration circuits (Figure C2) will be achieved by our planned increase in wafer throughput (Appendix B - Figure B1).

We expect the learning curve to be steeper than mature silicon technologies because techniques acquired from silicon experience will be applied to GaAs. Some examples of these are: extensive use of statistical process control; operator training; use of silicon processing equipment; robust circuit designs; process team meetings including process, design, and test groups; and extensive failure mode analysis.

Data Collection and Analysis

In the next two quarters, we will expand and refine the data collection system. We expect to have sufficient data after one quarter to begin to identify yield limiting steps. At that point we

can layout specific yield improvement tasks.

Figure C3 indicates the methodology use for the yield improvement plan. All key in-process parameters (geometrical and electrical) such as mobility, doping, line widths, and thicknesses are measured at critical operations. Statistical process control limits are implemented at each process step for two purposes. First, they establish the process capability and second, they provide a means to determine if the process has drifted out of control.

Process control monitors (PCMs) are tested after wafer fab to obtain device properties such as threshold voltage, current, transconductance, and resistance. Use of PCMs enables rapid feedback for process improvements in addition to guaranteeing compliance with process and device design specifications on all foundry lots. Details of the PCMs are described in the attached Design Rules.

Parametric, yield, and D_oY_o maps will be established at DC wafer probe. This will be the basis for the Failure Mode Analysis (FMA) activity which will link circuit results to device results and process and material parameters. All this information will be used to update both circuit and device models as well as the yield model.

The tasks to execute this methodology are shown in Table C1. Here the tasks have been divided between the material/process/test engineers and the product engineer. As can be seen in the table, the product engineer will be the key person who spans the entire process and is responsible for coordinating the flow and analysis of all the data.

Yield Model

Murphy's yield model will be adapted for establishing and projecting the relationships between chip area and yield using visual test, and FMA data. Since the model enables us to project yields for VLSI circuits based on smaller chip sizes, we will be in a position to design chips to accomplish yield objectives using data obtained from the demonstration vehicles on PT-1 and PT-2.

The three parameter yield equation $Y = Y_o/(1 + D_oA)^{1/\lambda}$ (where D_o is the measured mean value of the defect distribution (D/cm^2), λ = variance, Y_o is the measured fraction of wafer over which non-zero yield is obtained, Y is the yield, and A is the area of chip) will enable us to understand the inter-relationships between defects and parametric yields. The model will be validated for GaAs technology.

Demonstration Vehicles

We will determine baseline yields and D_oY_o for the pilot line by utilizing initially the 256 bit SRAM on both PT-1 and PT-2 reticle sets. In addition, the 6x6 multiplier and 4 bit adder will be used to establish logic circuit yields. We will migrate to larger demonstration vehicles for yields and D_oY_o monitoring as chips of higher levels of integration are fabricated.

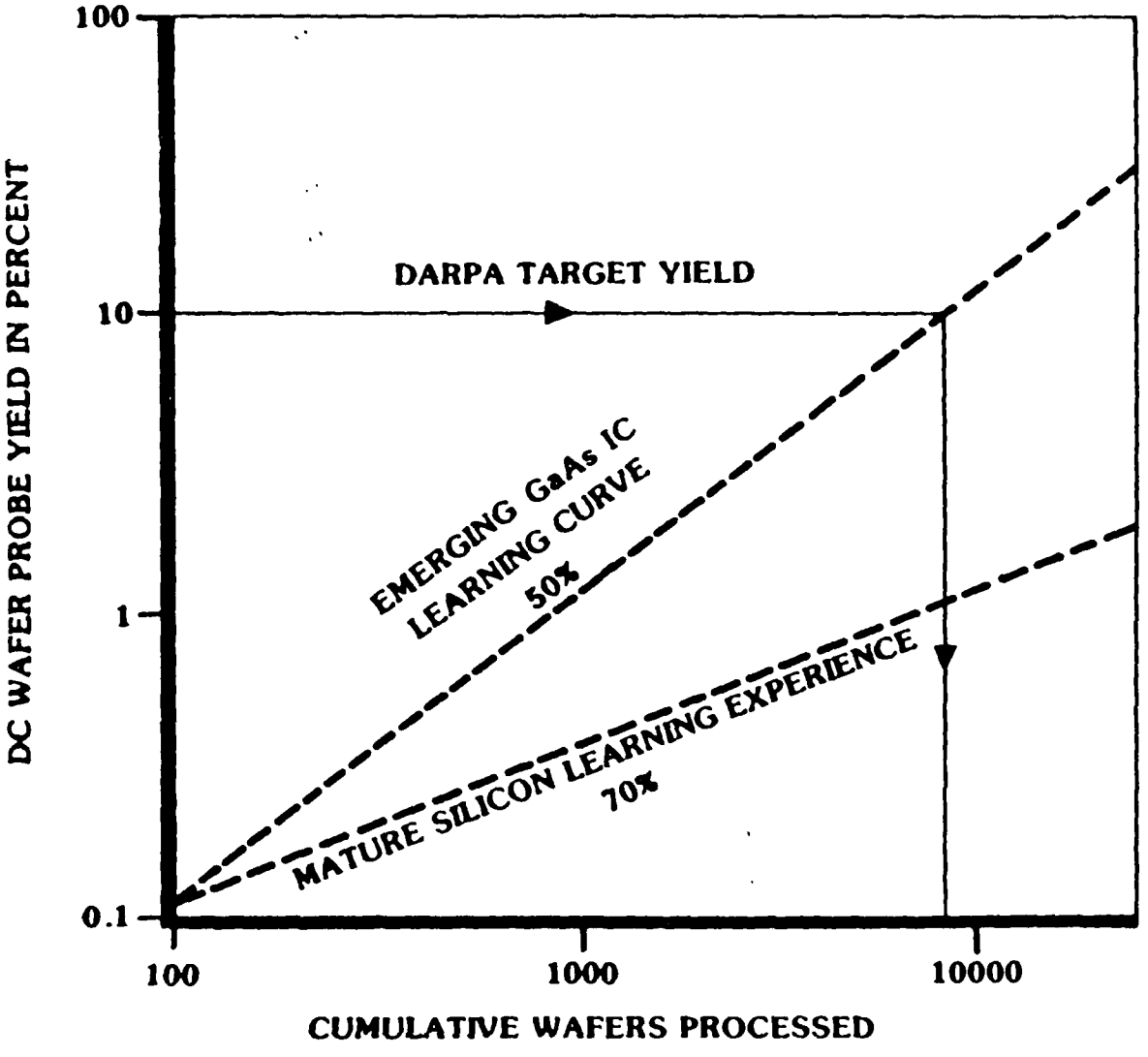
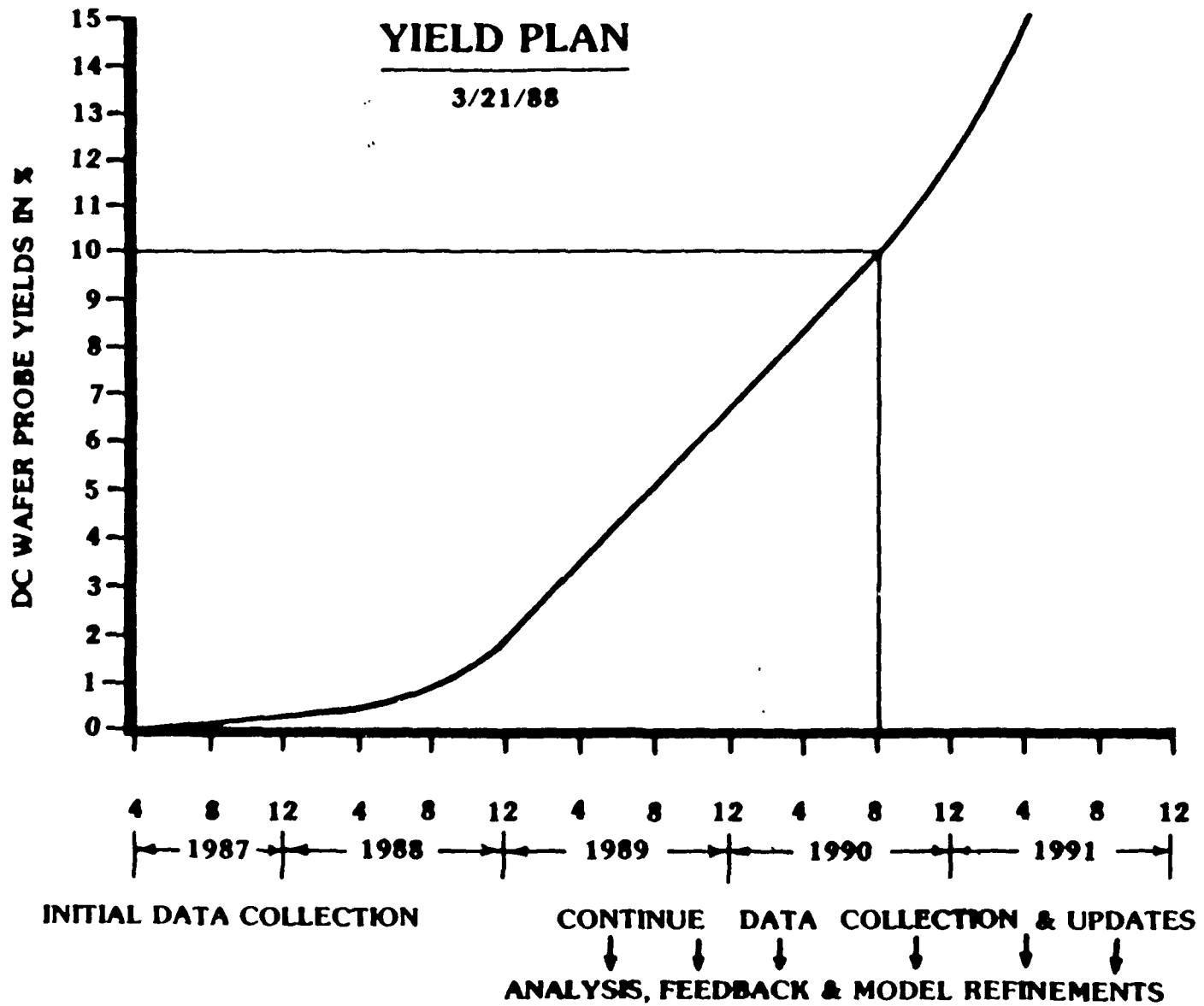


Figure C1. Expected Yield (5000 Equivalent Gates) Increases as Cumulative Volume Increases. The GaAs Technology Will Benefit from Extensive Silicon IC Experience.


YIELD PLAN
3/21/88
DC WAFER PROBE YIELDS IN %
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
4 8 12 4 8 12 4 8 12 4 8 12 4 8 12
1987
1988
1989
1990
1991
INITIAL DATA COLLECTION
CONTINUE DATA COLLECTION & UPDATES
ANALYSIS, FEEDBACK & MODEL REFINEMENTS

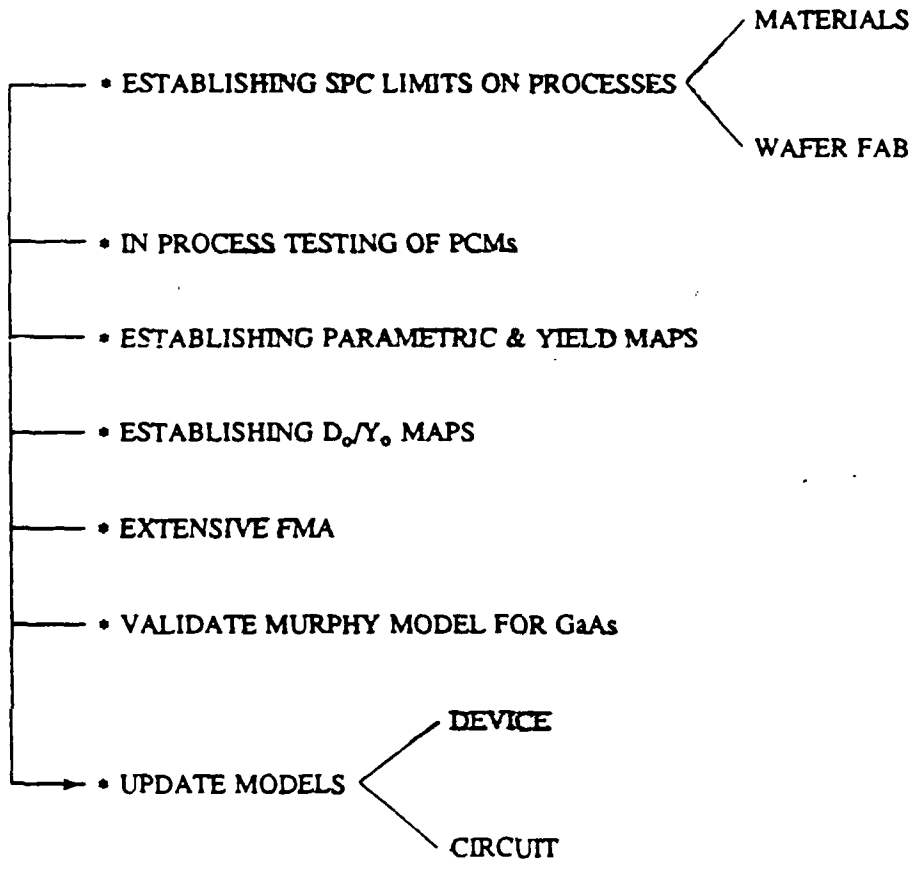


Figure C3. Yield Methodology

TABLE C1

Yield Evaluation Tasks

DATA & YIELD ANALYSIS

- MATERIALS/PROCESS/TEST ENGINEERS
- * PRODUCT ENGINEER

MATERIALS

- ESTABLISH STATISTICAL PROCESS CONTROL (SPC) PROCESS LIMITS
- COLLECT PARAMETRIC & YIELD DATA
- * CORRELATE MATERIALS TO DEVICE RESULTS

WAFER FAB

- ESTABLISH SPC PROCESS LIMITS
- COLLECT IN-PROCESS PARAMETRIC & YIELD DATA
- * CORRELATE REQUIRED TO ACTUAL PROCESS LIMITS

PCM TESTING

- ESTABLISH DEVICE LIMITS
- COLLECT PCM PARAMETRIC & YIELD DATA
- * CORRELATE PROCESS TO DEVICE RESULTS

CIRCUIT TESTING

- GENERATE MAPS & STATISTICS
- - FUNCTIONAL YIELDS
  - PARAMETRIC DATA
- INPUTS FOR MURPHY MODEL
- * VALIDATE MURPHY MODEL
- * CORRELATE CIRCUIT TO DEVICE RESULTS

FAILURE MODE ANALYSIS

- INVESTIGATE FAILURE MODES
- * INPUT FOR FAILURE MODE ANALYSIS

*Activities coordinated by Product Engineer

APPENDIX D

Industry Survey of High Speed Packages

(A. D. Butherus, K. J. Brady)

Introduction

The contract Statement of Work says "Contractor shall survey the industry for appropriate high speed packages with Input/Output (I/O) ranging from 20 pins to 230 pins. The survey shall be fully documented in contract Semi-Annual Technical Reports." We shall interpret "appropriate high speed" term as meaning appropriate to the chips being designed for the contract, i.e. for clock speed of 200 MHz.

There are hundreds of packages available in the marketplace, but very few have the necessary combination of high-speed capability and high I/O count. Typically, a high-speed chip and its package are designed serially, with the package designed to the specific geometric and electrical requirements of the chip and also the system requirements of the circuit.

In contrast to the ideal situation described above, where the package is custom-designed to the chip and its application, this contract requires that we locate suitable high-speed packages in the marketplace in which the demonstration circuits are to be delivered. Inherent in such a strategy is the need for minimizing the performance loss possibly associated with non-custom packages.

To find the optimum commercial packages, we will consider only those packages whose characteristics are consistent with high-speed operation, and will organize the package data of this survey into areas of concern for high speed operation. A candidate package for one of our deliverable circuits can thus be analyzed for suitability by determining the performance risk associated with each area of concern listed. An overview of the areas of concern is shown in Figure D-1.

We have divided the packaged circuit into five areas of concern:

I. **Chip-to-Cavity Match** The chip obviously has to fit into the cavity, but if the cavity is too large, there is an inductance penalty in the overly-long wire bonds required.

II. **Electrical Characteristics of the Package Body** The signal rise and fall times for the circuits in the contract typically correspond to bandwidths of ~1.3 GHz, so the package must be able to transmit these signals out to the external leads at these frequences (see Figure D-2). Typically the package body should incorporate ground planes, controlled impedance signal lines, and interspersed ground and signal lines to prevent crosstalk. The performance degradation of candidate packages which don't have these design features will have to be determined on a case-by-case basis for use in the contract. Additionally, the ability to connect by-pass capacitors and terminating resistors to the package I/Os is useful for minimizing noise.

III. **External Connection Geometry** Generally, packages for IC chips fall into two broad families, through-hole mount and surface mount. The through-hole family contains the DIPs and the pin grid arrays, (PGAs). The surface mount family contains Small Outline Integrated Circuits (SOICs), chip carriers and flatpacks. Examples of these package types are shown in Figures D-3 - D-12. The through-hole mount package pins present large discontinuities where the package pin meets the board. This large discontinuity limits the use of these packages to applications to bandwidths below 500 MHz, less than half the required bandwidth for use in this contract work.

In the surface mount family the SOIC is a molded plastic package not well suited for

high frequency applications. The chip carriers and the flatpacks are the package styles best suited for high frequency applications. The flatpacks offer the least discontinuity at the package/board interface and therefore is the style most used.

IV. **Thermal Characteristics** High-speed in ICs is often associated with more power dissipation than comparable circuits operating at lower speeds, and the heat must be removed to maintain junction temperatures at low enough levels consistent with noise margins and reliability.

V. **Associated Components** All else being equal, a package system consisting of test fixturing, burn-in sockets and carriers is preferred. This aspect is often overlooked, but the best package in the world has to be connected somehow to a test system for evaluation. These system components are often as expensive and time consuming to design and make as the package itself.

The relative importance factors affecting package choice for a give chip are shown schematically in Figure D-13.

THE PACKAGE SURVEY

Several manufacturers offer open-tooled packages with controlled impedance signal lines for high frequency applications. The manufacturers and the packages they offer are listed in Table D-1. The pin counts offered cover the range from 20 to 164 with signal line counts from 8 to 148. Listed at the bottom of Table D-1 are several package from Mini Systems Inc. (MSI), these packages do not have controlled impedance signal lines, but these packages have been tested and found to be useful at frequencies up to 2 GHz.

Two points are obvious from the entries in Table D-1. First, the packages at the top of the table have been designed to have a characteristic impedance, Zo=50Ω. The second point is that the entries in the table do not cover the high end of the pin count range. For example, the Casino Test Chip has 177 signal lines, therefore, none of the packages listed could accommodate this chip.

Devices designed to operate with 75Ω characteristic impedance signal lines would dissipate less power. Consequently, the three manufacturers listed at the top of the Table D-1 were asked about the possibility of designing packages with 75Ω characteristic impedance transmission lines. The two ceramic manufacturers, Interamics and TriQuint answered that they felt that such high impedance packages would not be manufacturable. The reason for this is the high dielectric constant of the alumina ceramic, E_r = 9.6, and the relation that governs the characteristic impedance Zo of a transmission line:

$$Zo = \sqrt{\frac{L}{C}} = \frac{[\text{Geometric Factors}]}{\sqrt{E_r}}$$

where L = inductance per unit length, C = the capacitance per unit length, and E_r = the dielectric constant. To produce a package with 75Ω characteristics impedance signal lines would require pushing the geometric factors to values which are impractical for manufacture. Only Augat-Microtic using polyimide with $E_r \leq 3.8$ would attempt to fabricate packages with 75Ω impedance signal lines. Some samples of packages with 75Ω signal lines have been ordered from Augat-Microtic but have not yet been delivered and are in fact six months late

from the promised delivery date, indicating some difficulty in achieving the required 75Ω characteristics.

Since packages with controlled impedance signal lines are not available with sufficient signal line count, the second option is to keep the length of these signal lines to a minimum. The length of these lines should be less then $\frac{\lambda}{4}$ where λ is the signal wavelength. An estimate of the signal wavelength can be obtained from the signal rise time (see Figure D-2). The equivalent frequency is approximately 1.3 GHz and this leads to a signal wavelength of approximately 7.5 cm; thus $\frac{\lambda}{4} \approx 1.9$ cm. Therefore, the second choice in selecting packages for this application is to choose those packages with signal line lengths less than 1.9 cm.

The viability of this second option is demonstrated by the experience with the MSI packages listed at the bottom of Table D-1. These packages do not have controlled impedance signal lines, yet they have been shown to be useful up to frequencies of 2 GHz. The reason for this is the packages are very small, and the length of the signal lines is very small compared to the signal wavelength.

There are two types of packages that have pin counts that cover the high end of the required range, the pin grid arrays (PGA's) and the fine pitch leaded chip carriers or flatpacks. The PGA's are through hole mount packages and as noted earlier are not used for high frequency applications because of the severe impedance discontinuity at the pin/board interface. The other type of package, the leaded flatpack, is the choice for high frequency applications. All of the entries in Table D-1 are leaded flatpacks, whether standard lead pitch, .050", or fine pitch with lead center ≤ .050".

Table D-2 is a list of available production tooled leaded flatpacks with pincounts above the 148 signal lines of the packages listed in Table D-1. These packages do not have dedicated ground and power lines so all lines are potentially available for signals. All the lines on these packages satisfy the line length requirement noted above. The converse of the fact that all lines are potential signal lines is the fact that these packages do not have built-in ground and power planes. The lack of these built-in planes will mean significantly increased cross-talk on the signal lines and significantly increased inductive noise on the DC lines. The obvious way to reduce these problems is to intersperse among the signal lines as many as possible ground and power lines. The ideal would be a ground-signal-ground line arrangement. Table D-2 lists the body size, the lead pitch and the cavity size for the flatpack packages. The packages listed are all fine pitch, with lead pitch of .020" or .025". Also listed is the information on the availability of carriers and (low frequency) sockets for the packages. Carriers and sockets are considered necessary support elements to the chip packaging operation; if they do not exist, they will have to be developed. It is not possible to deliver devices in fine pitch flatpacks without carriers and sockets.

Listed at the bottom of Table D-2 is a 256 I/O flatpack designed by AT&T for the EMSP project. AT&T has given permission to use this package and its supporting carriers and sockets in the DARPA project. The package has been production tooled and parts are on hand. The supporting carriers and sockets have been developed and will be available starting in May, 1988.

In addition to the availability of the support elements the EMSP has two electrical advantages.

The first is that the package does have a built-in ground plane and although it is not ideally located, this ground plane still offers significant reduction in signal cross-talk. The second is that with the highest available I/O count the package offers the best opportunity of distributing DC lines among the signals.

THE FOLLOWING SECTION DESCRIBES HOW THE RESULT OF THE INDUSTRY SURVEY AND THE ANALYSIS OF THE HIGH SPEED REQUIREMENTS DETAILED HERE WERE USED TO SELECT PACKAGES FOR THE CONTRACT.

RECOMMENDATIONS

The 24 signal, 44 total I/O package from TriQuint was selected for use with the PT-1 chips. This is a true high frequency package, designed with 50Ω signal lines and provision for mounting bypass capacitors on the package. It is recommended that this package be used for the final 4K SRAM. The package is ceramic can be hermetically sealed. A photograph of this package is shown in Figure D-14. The body of the package is .650" sq. with leads on .050" pitch. Carriers are not necessary for packages with this pitch. Low frequency sockets are available for this package. A high frequency test fixture is also commercially available to fit this package. Some preliminary tests have shown that this test fixture performs well to frequencies beyond 1GHz, certainly sufficient for the present application.

Another important feature of this package is that it is designed to accommodate high power chips. The die attach substrate is a copper/tungsten composite that is coexpansive with the ceramic body but has a thermal conductivity an order of magnitude higher than ceramic. This high conductivity die mount is not the total solution to the thermal management problem for a high power chip but it is an important contribution to the solution.

The 64 signal, 88 total I/O package from Interamics was selected for use with the PT-2 logic chips. Again, this is a true high frequency package with 50Ω signal lines, some built in bypass capacitance and the high thermal conductivity die attach substrate. This package is recommended for use with any of the logic chip deliverables. A photograph of this package is shown in Figure D-15. This package is also ceramic with provision for a hermetic seal. The package body is .500" sq. with 23 leads per side, at .020" pitch. (The two leads that surround each of the four corners are tied together, hence the designation 88 rather than 92 total I/O.) This is a fine pitch package, but the carriers and sockets are not available, neither are high speed test fixtures. These support elements will have to be developed.

The 256 I/O fine pitch leaded flatpack designed by AT&T for the EMSP project appears to be the best available package for the high pin count logic devices. A photograph of this package is shown in Figure D-16. This package is not ideal but it does have several advantages, namely a built-in ground plane, spare I/O for signal isolation, and available carriers and sockets. The principal drawback to this package is that the die cavity (.560"sq.) is too large for the expected size of the Casino Test Chip, .320"sq. This same problem exists to a greater or lesser extent for all of the high pin count packages however. The high frequency test fixtures for this package will have to be developed, but this same development would be required for any of the high pin count packages. The 256 I/O package does not have a high thermal conductivity die attach substrate, but again neither do any of the other high pin count packages. This adds an important resistance in the heat flow path but it doesn't preclude a solution to the thermal management problem.

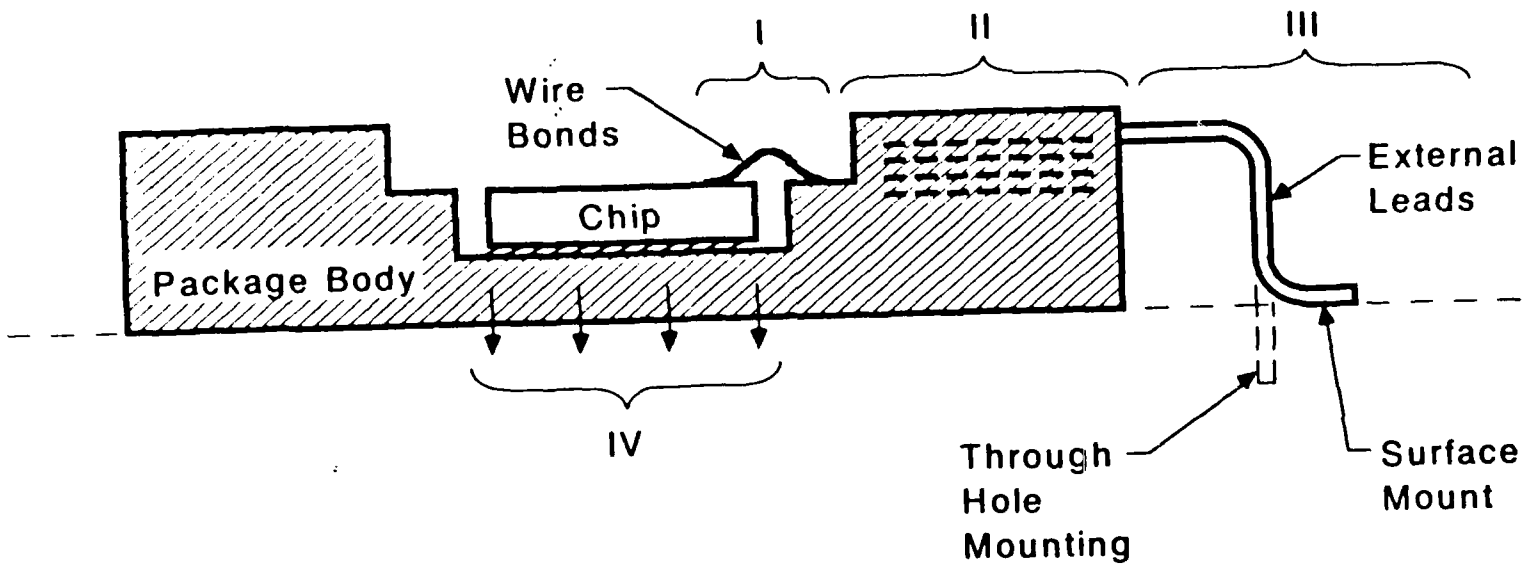
A request for approval to use the 256 I/O EMSP will be submitted to the COTR.

TABLE D-1

Packages with Controlled Impedance (Zo = 50Ω) Signal Lines

VENDOR	I/O COUNT (SIGNAL/TOTAL)	PACKAGE BODY MATERIAL	CAVITY SIZE (in)	COMMENTS
INTERAMICS	28/32	ALUMINA	.190X.250	
	64/88	"	.250X.250	MAYO DESIGN
TRIQUINT	8/20	ALUMINA	.060X.060 (CHIP)	NO CAVITY, PERFORMANCE VERIFIED TO 18GHz
	24/44	"	.130X.130	PROVISION FOR MOUNTING BYPASS CAPACITORS.
	64/132	"	.210x.210	PROVISION FOR MOUNTING BYPASS CAPACITORS.
AUGAT - MICROTEC	64/88	POLYMIDE	.250X.250	MAYO DESIGN
	116/132	"	.400X.400	PROVISION FOR MOUNTING BYPASS CAPACITORS.
	148/164	"	.400X.400	PROVISION FOR MOUNTING BYPASS CAPACITORS.
Additional Packages Usable in High Frequency Applications				
MSI	20/20	ALUMINA	.140X.140	PACKAGE BODY .270"SQ.
	32/32	"	.265X.265	" " "
	64/64	"	.360X.360	PACKAGE BODY .640"SQ.
	84/84	"	.300X.300	" " "

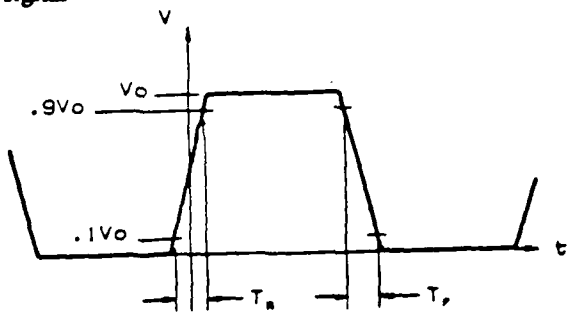
TABLE D-2						
High I/O Count Leaded Flatpacks						
I/O #	Manufacturer	I/O Pitch in.	Body Size in. (SQ)	Cavity Size in.	Carrier/Burn-In Socket	Comments
152	NTK	.020	.840	.380x.380	YES	Open Tooled, No Ground or Power Planes
172	NTK	.020	.940	.380x.380	YES	
172	KYOCERA	.025	1.150	.380x.380	NO	
196	KYOCERA	.025	1.350	.410x.410	NO	
256	NTK	.020	1.380	.540x.550	YES	
256	KYOCERA	.020	1.480	.500x.500	NO	
256	NTK	.020	1.450	.560X.560	YES	AT&T design, Ground and Power Planes



Cross Section Of Chip Assembly, Showing Critical Areas For High-Speed Suitability. (Lid Omitted For Clarity)

FIGURE D-1:

To obtain a signal frequency from a signal with a known signal rise time T_r and signal fall time T_f, one compares the signal



to a sine wave with the same amplitude and the unknown frequency f,

$$V(t) = \frac{Vo}{2} [1 + \sin 2 \Pi ft]$$

For simplicity assume $T_r = T_f$, then equating the sine wave value to the signal value at $t=T_r/2$ yields

$$.9Vo = \frac{Vo}{2} [1 + \sin \Pi fT_r]$$

which has the solution

$$f = \frac{\sin^{-1}(.80)}{\Pi T_r} = \frac{.295}{T_r}$$

For a signal with a rise time T_r = 225 ps, the frequency is

f=1.3 GHZ

Then, from the wavelength/frequency relationship

$$\lambda f = \frac{C}{\sqrt{E_r}}$$

where λ is the wavelength, C is the speed of light and E_r is the relative dielectric constant for the package body material. For a ceramic package E_r = 9.6, then

$$\lambda = 7.4cm$$

FIGURE D-2:

The calculation of the signal frequency and wavelength from the signal rise time

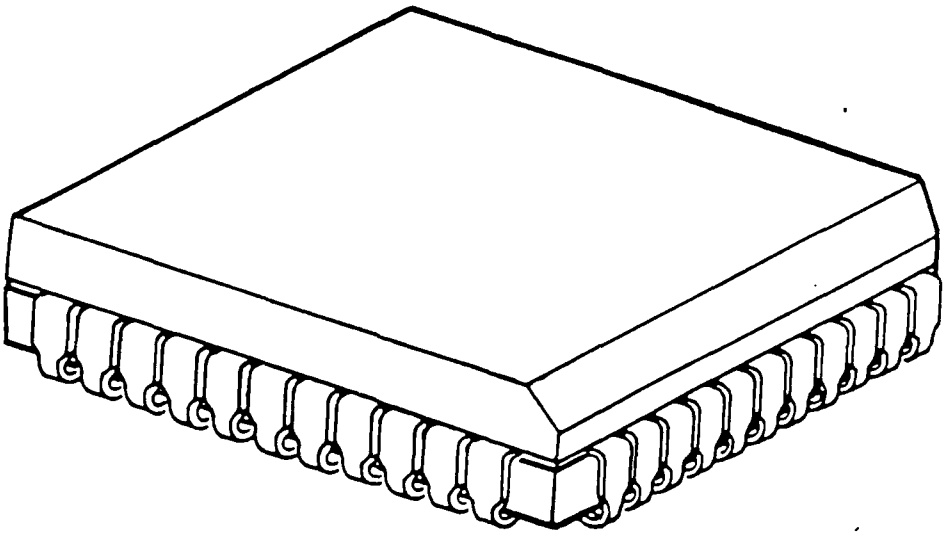


FIGURE D-3: Post Molded Plastic Chip Carrier

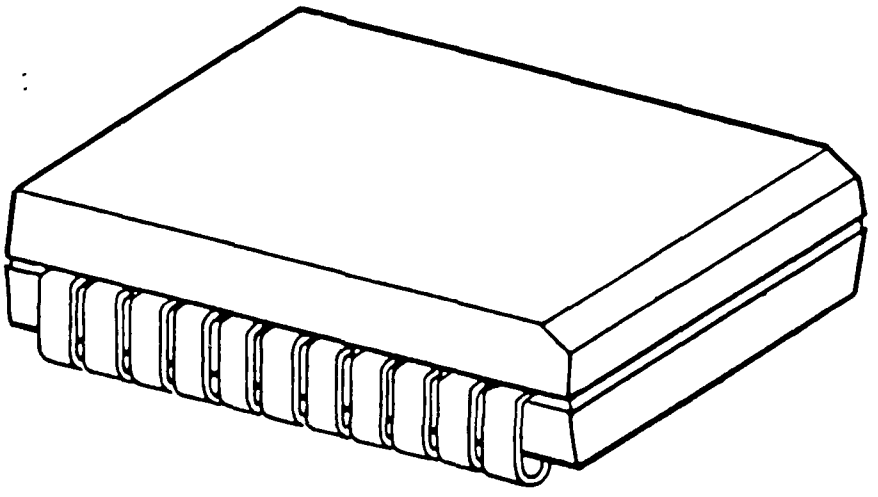


FIGURE D-4: SOJ (Small Outline J Lead)

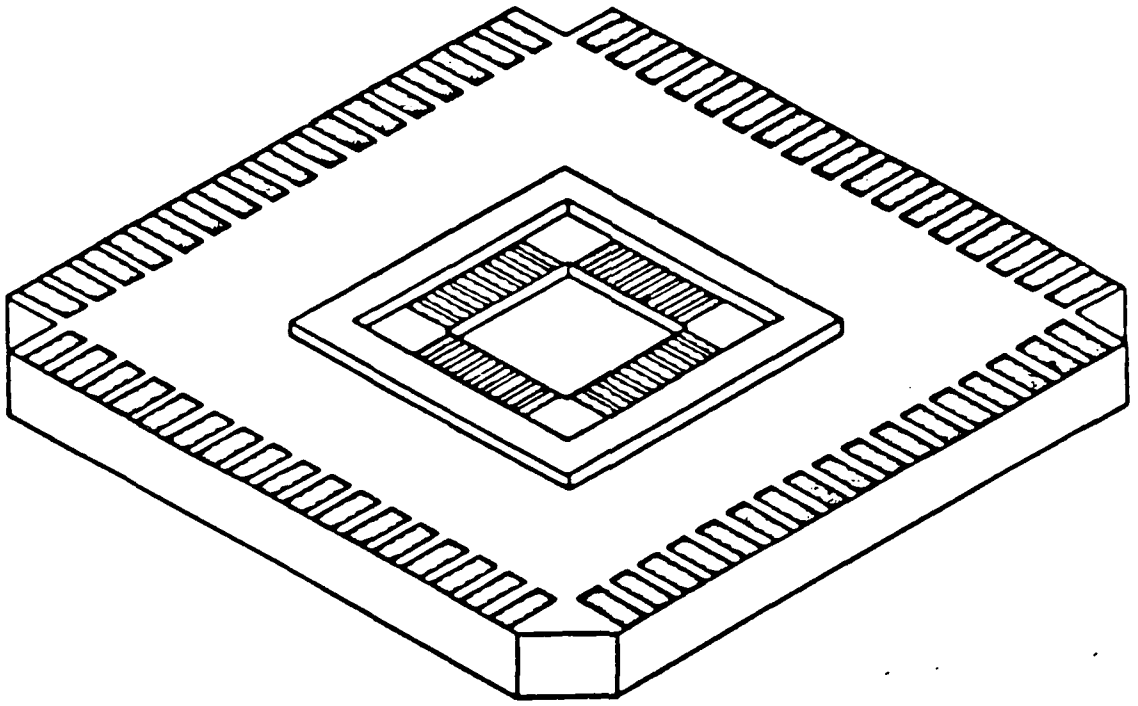


FIGURE D-5: Leadless Ceramic Chip Carrier

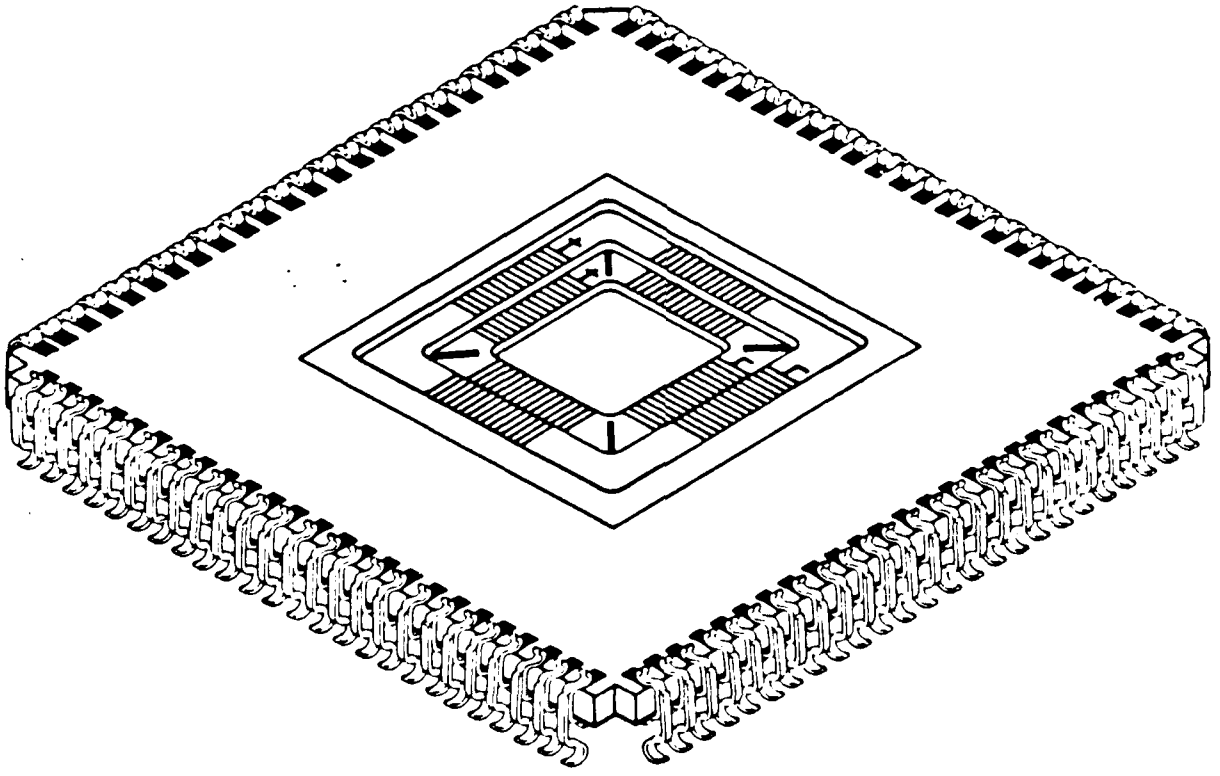


FIGURE D-6: Leaded Ceramic Chip Carrier

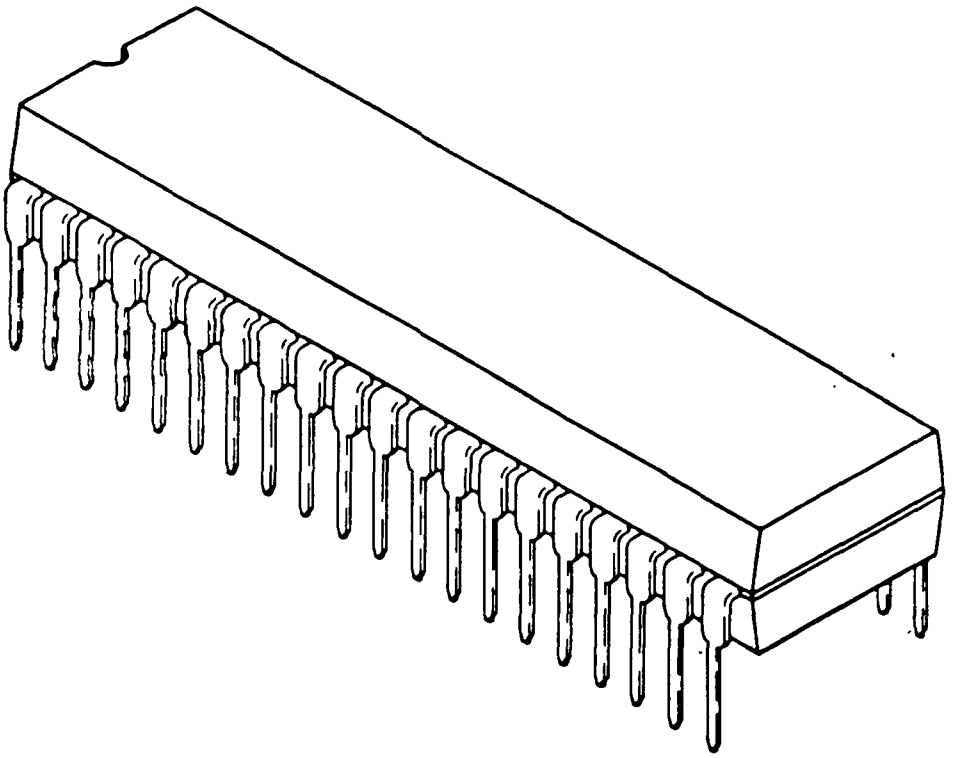


FIGURE D-7: Post Molded Plastic DIP

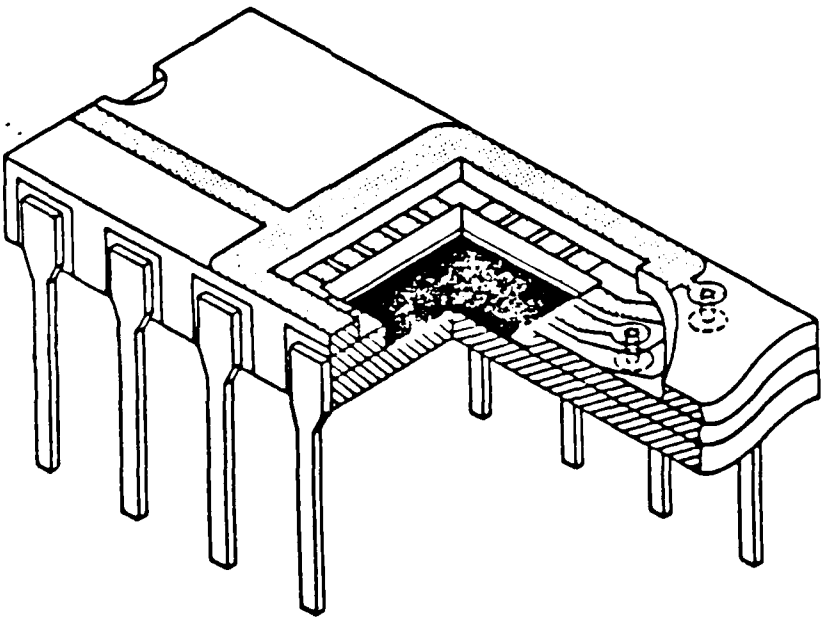


FIGURE D-8: Ceramic DIP

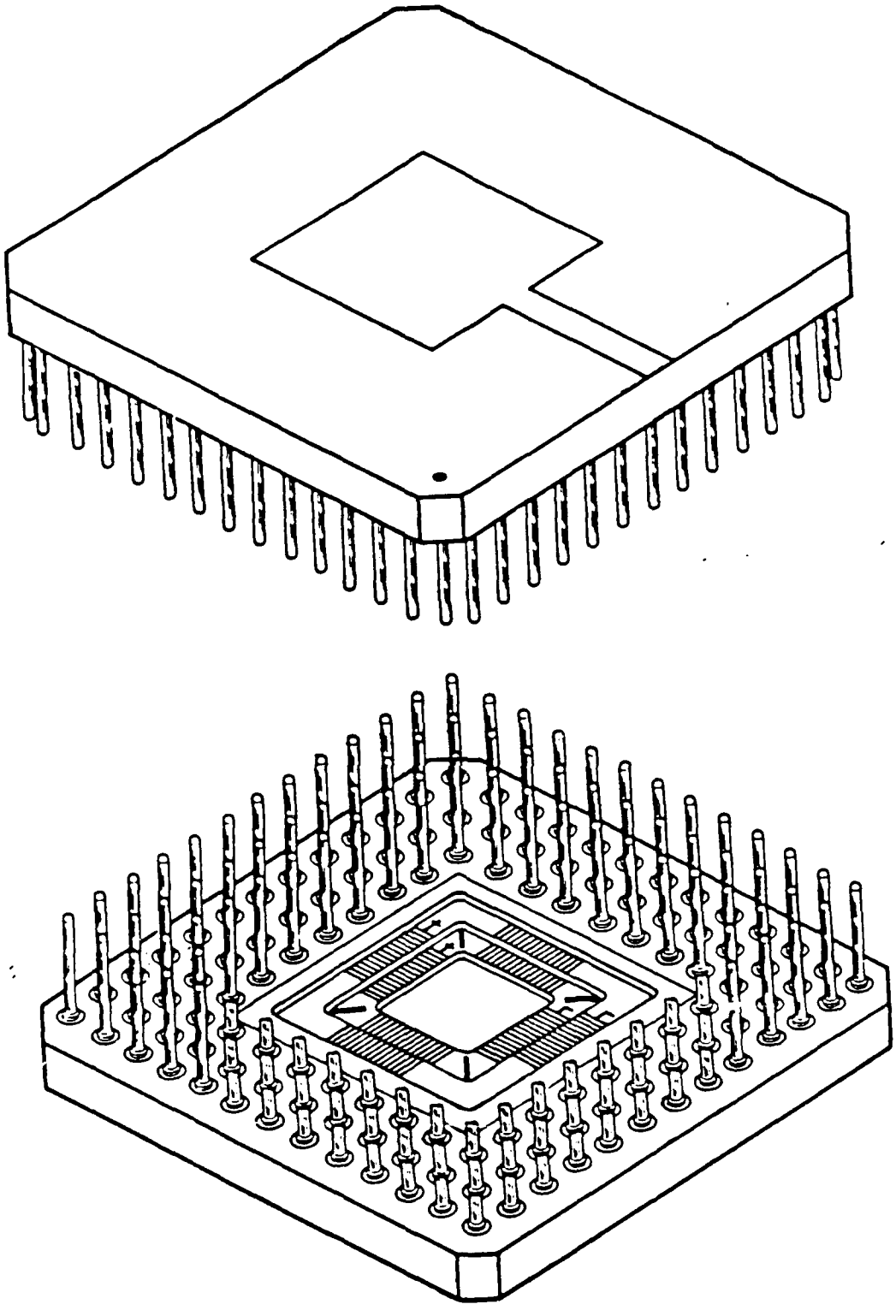


FIGURE D-9: Ceramic Pin Grid Array

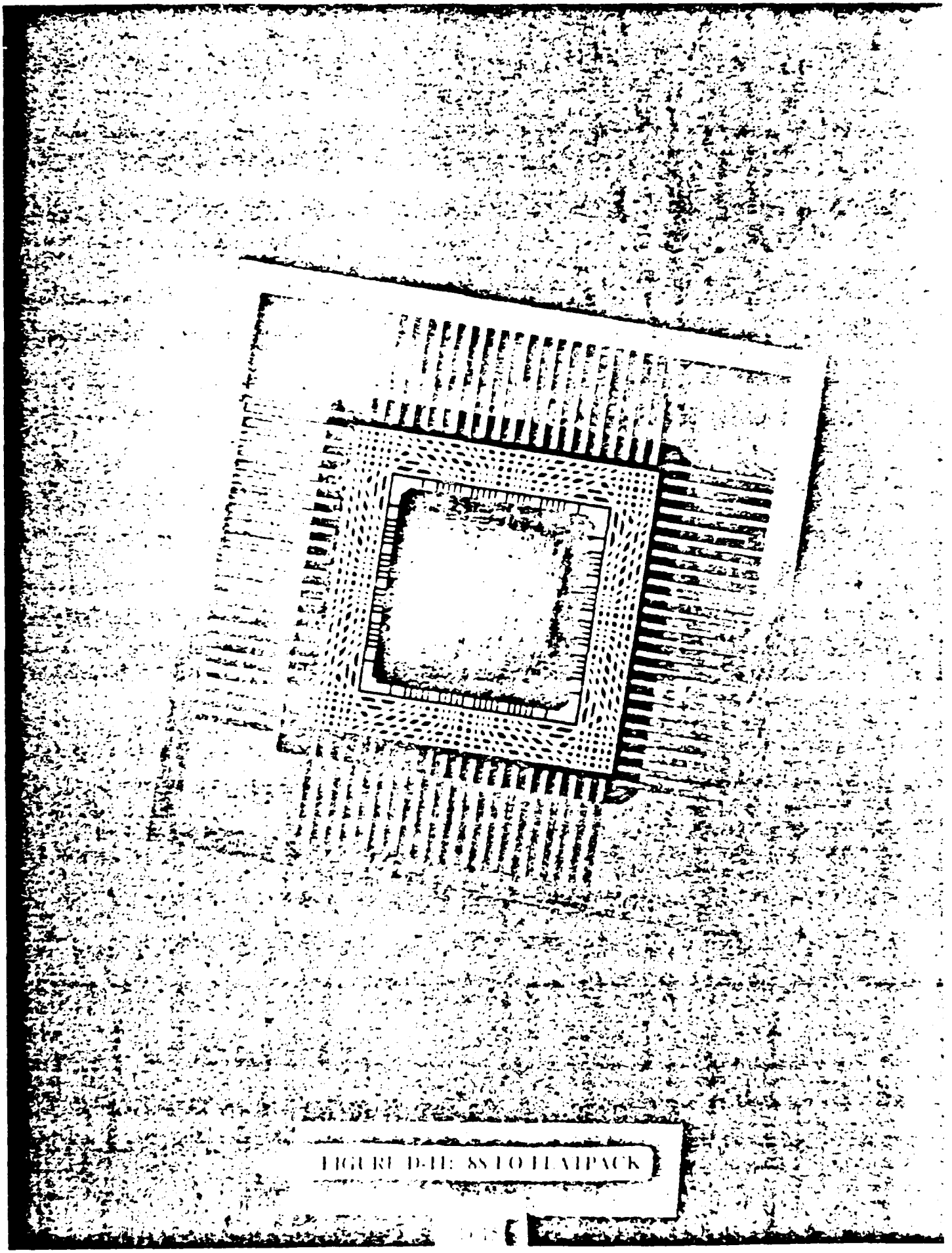


FIGURE D-11. 8S TO FLATPACK

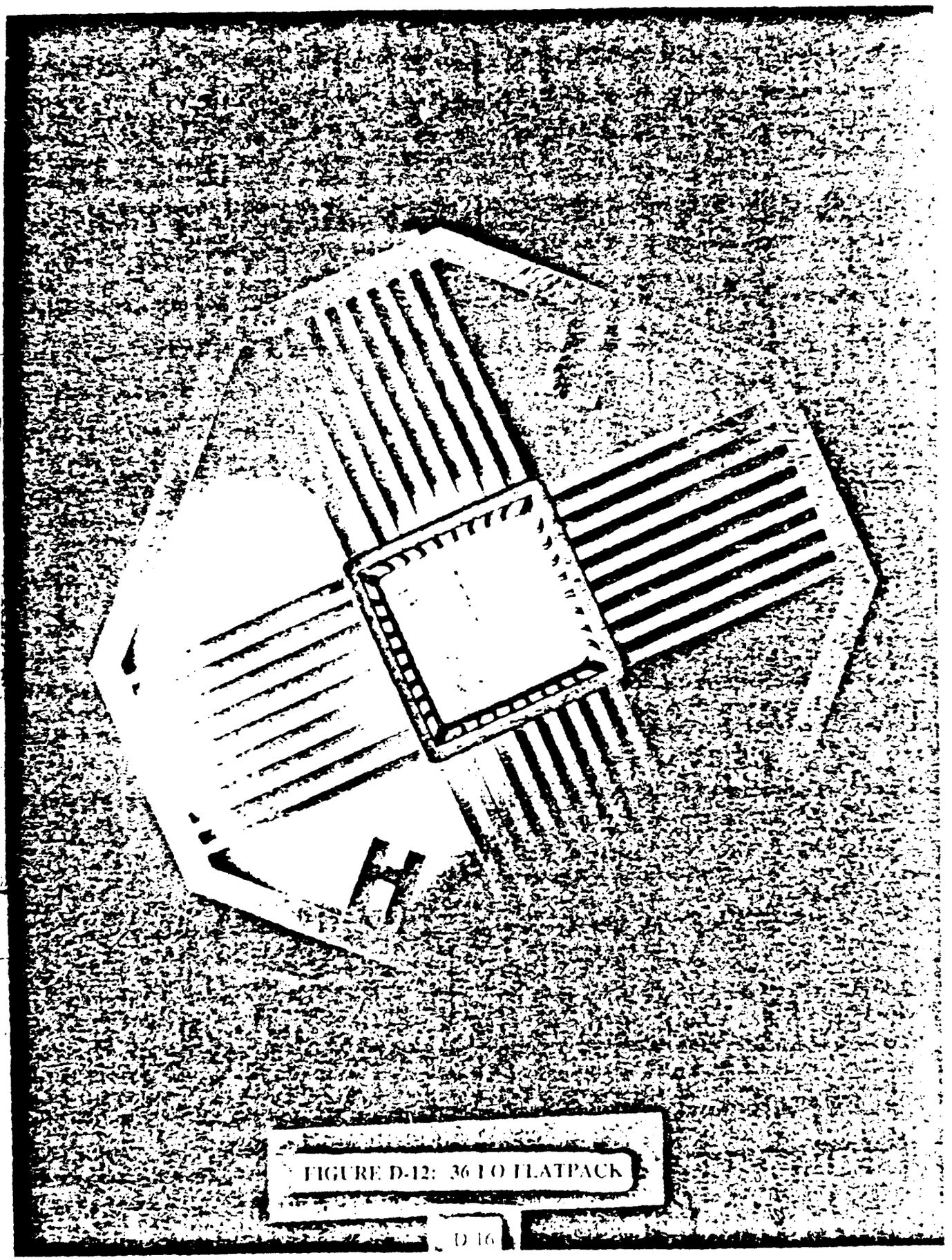


FIGURE D-12: 36 I/O FLATPACK

HIGH-SPEED PACKAGE SELECTION PROCESS

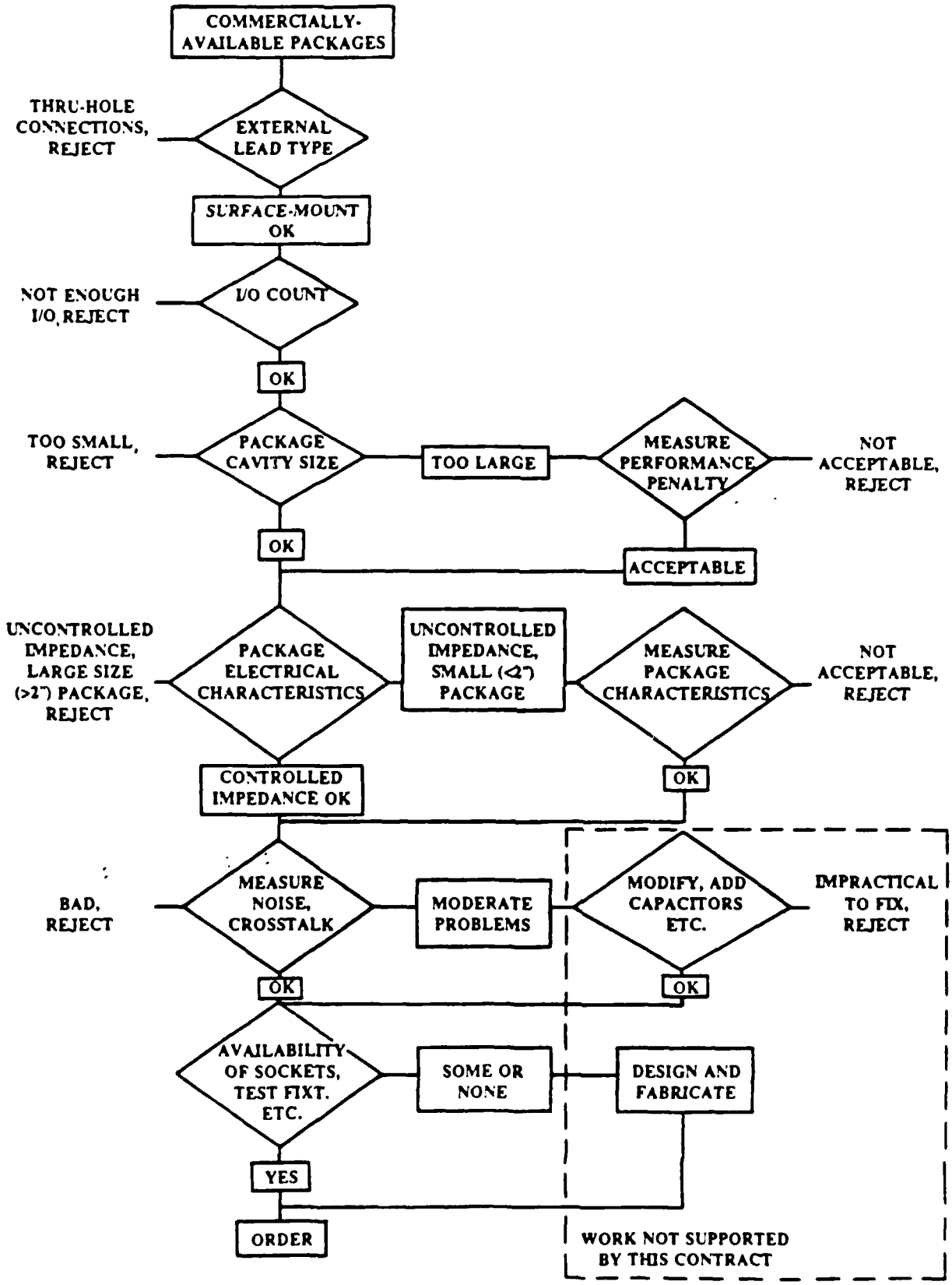


FIGURE D-13:

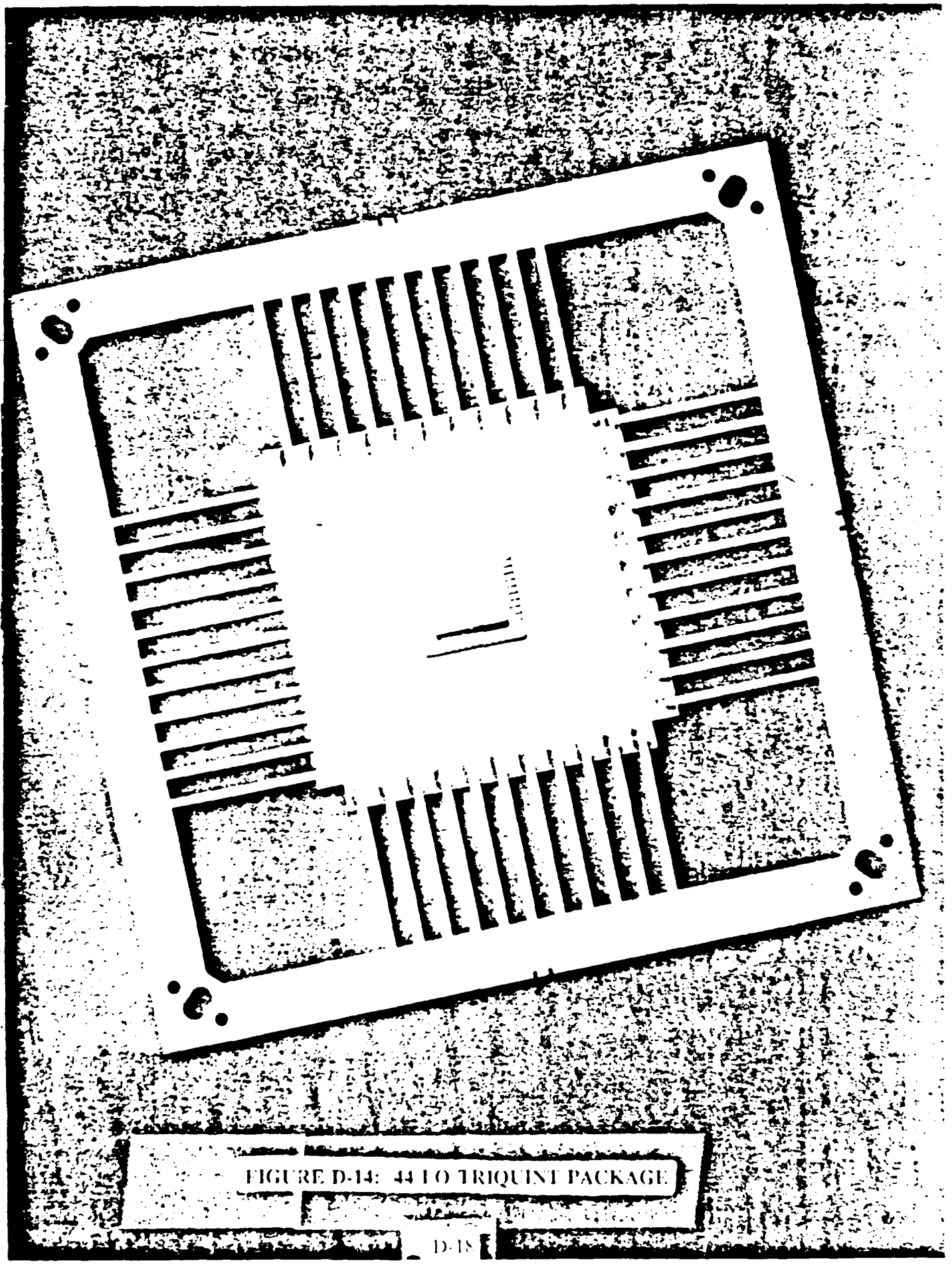


FIGURE D-14: 44 I/O TRIQUINT PACKAGE

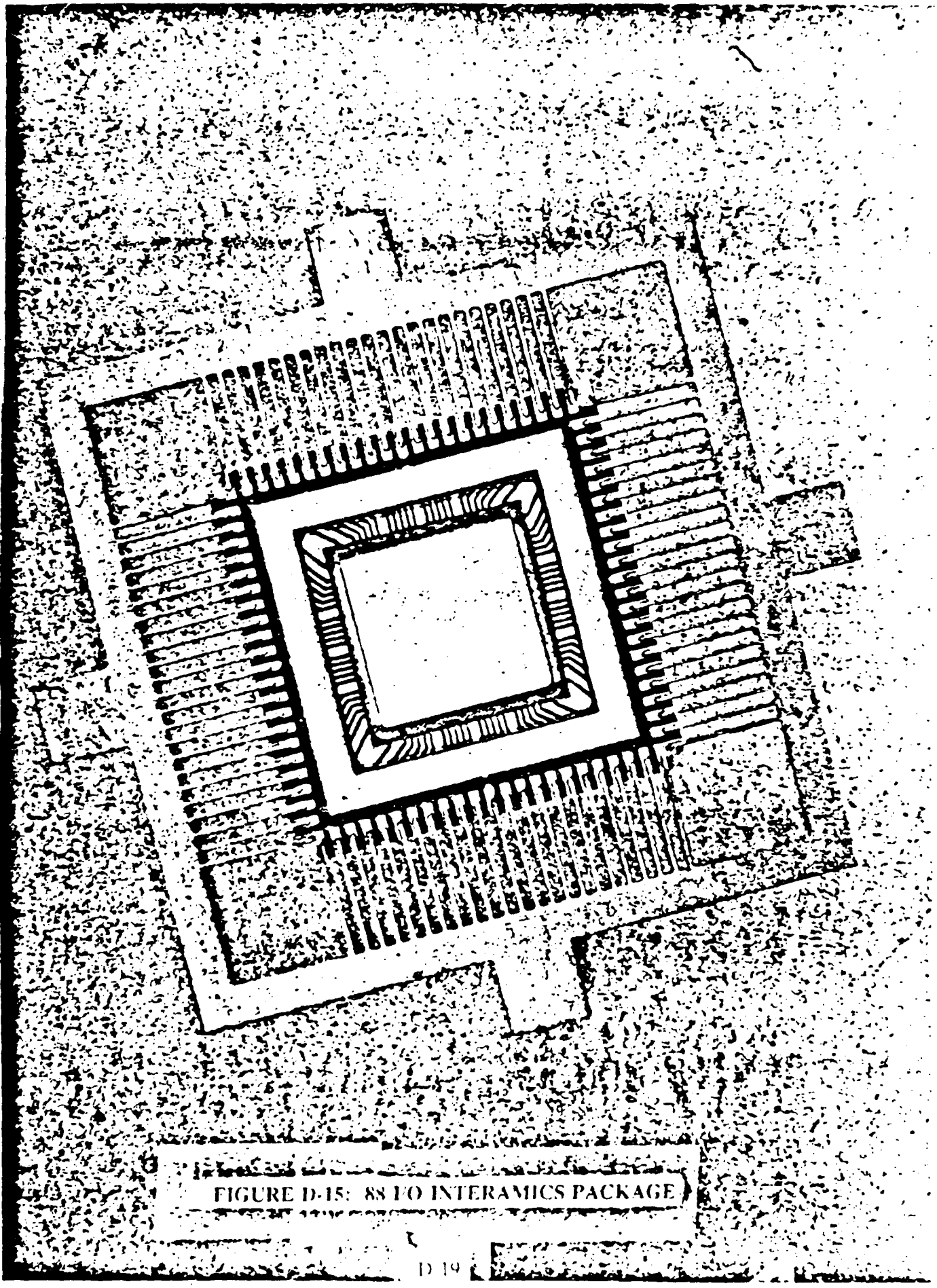


FIGURE D-15: 88 I/O INTERAMICS PACKAGE

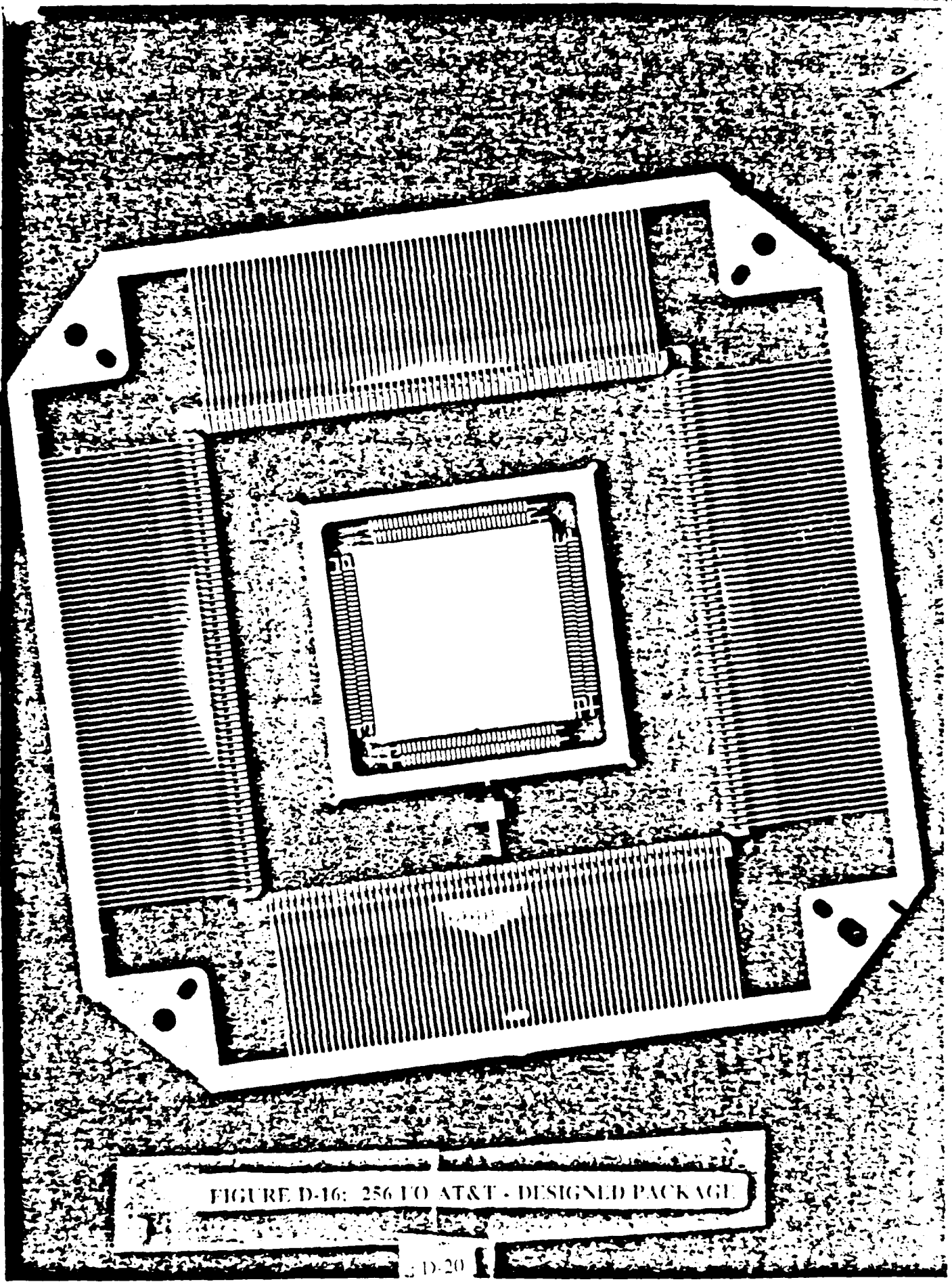


FIGURE D-16: 256 I/O AT&T - DESIGNED PACKAGE

END

DATE

FILMED

DTIC

9-88